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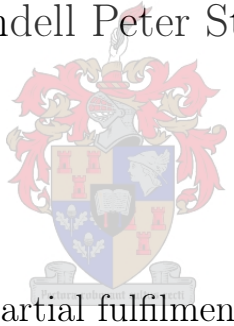
A comprehensive simulation based methodology for optimal design of a PMSM drive

by

Cundell Peter Statt



Thesis presented in partial fulfilment of the requirements for the degree of Master of Engineering (Electrical and Electronic) in the Faculty of Engineering at Stellenbosch University

Study leader: Dr. Johannes M. Strauss

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Declaration

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Abstract

One of the biggest problems with regards to electric vehicles is range and charge times. Therefore, the efficiency of the electric drive train is of utmost importance. This has resulted in the common use of three-phase brushless permanent magnet synchronous machines. Due to the DC nature of batteries, a three-phase motor drive is needed, which is the focal point in this thesis.

Although efficiency is one of the key design focuses, a compromise has to be made between this, cost and weight. A compromise is never an easy task to perform however, the more information available, the more accurate of a choice can be made. Thus, a method using simulation was developed aiding in the process of setting the minimum MOSFET specifications. From this, the losses of each MOSFET in the selection can be determined through a second Simulink simulation.

Typically the choice of switching component would now be made with the thermal effects being a secondary design process. However, placing the thermal aspect at the forefront of the design can result in a large savings in cost and weight, due to a reduction of cooling requirements. For this reason, a method using computational thermodynamics was developed to allow multiple design revisions to be tested and optimised.

To further aid in the choice of the optimal MOSFET, each MOSFET in the selection is simulated in the thermal model using the previously determined losses. The maximum temperature for each MOSFET is determined, clearly indicating which MOSFETs are the thermally optimal choice.

The design and construction of a 5 kW permanent magnet synchronous machine drive is completed. From this, the accuracy of the simulations can be tested and confirmed. The drive is focused on lightweight vehicle applications such as the vehicle produced by the company Mellowcabs. Thus, simulations were run focusing on the optimisation and improvement of their cooling method to reduce cost and weight. By doing this the benefits of placing the thermal aspect at the forefront of the design can clearly be seen.

Uittreksel

Een van die grootste probleme met elektriese voertuie is reikafstand en laaitye en daarom is die doeltreffendheid van die elektriese masjienaandrywing van die grootse belang. Dit het algemeen gelei tot die gebruik van driefase, borsellose, permanente magneet sinkroonmasjiene. Met batterye wat direkte stroom lewer word driefasemasjienaandrywing benodig. Dit is die fokus van hierdie tesis. Alhoewel benuttingsgraad een van die belangrikste fokuspunte van ontwerp is, moet daar 'n kompromie aangegaan word tussen benuttingsgraad, koste en gewig. 'n Kompromie is egter nie 'n maklike taak om uit te voer nie, maar met meer inligting kan 'n meer akkurate keuse gemaak word. Dus is 'n metode ontwikkel wat gebruik maak van simulasie om die minimum MOSFET spesifikasies vas te stel. Vervolgens kan die verliese van elke MOSFET in die keuse bepaal word deur 'n tweede simulasie. Gewoonlik word die keuse van skakelkomponente nou gemaak met die termiese aspekte as sekondere ontwerpsproses. Deur die termiese aspekte aan die voorpunt van die ontwerpsproses te plaas, kan dit lei tot groot vermindering in koste en gewig deur die vermindering in verkoelingsvereistes. Vir hierdie rede is 'n metode ontwikkel wat gebruik maak van numeriese termodinamika wat verskeie ontwerpswysigings toelaat om getoets en geoptimeer te word. Om verder te help met die keuse van die optimale MOSFET, is elke MOSFET in die keuselys gesimuleer in die termiese model deur gebruik te maak van die verliese wat voorheen bepaal is. Die maksimum temperatuur vir elke MOSFET is bepaal wat duidelik aandui watter MOSFET is die termies optimale keuse. Die ontwerp en konstruksie van die 5 kW permanente magneet sinkroonmasjienaandrywer is voltooi. Vervolgens kan die akkuraatheid van die simulasies getoets en bevestig word. Die aandrywing is gefokus op ligte motorvoertuig toepassings soos die voertuig wat vervaardig word deur die maatskappy Mellowcabs. Dus was simulasies gefokus op die optimering en verbetering van die verkoelingsmetodes om koste en gewig te verminder. Deur hierdie te doen is die voordele van die plasing van die termiese aspekte aan die voorpunt van die ontwerp duidelik.

Acknowledgements

I would like to extend my gratitude towards Dr JM Strauss for his guidance and support throughout this project.

I would also like to thank the team at Mellowcabs for the knowledge they shared with me and allowing me to use their equipment.

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Nomenclature

Variables

V_{TN}	MOSFET turn on voltage
V_{GS}	MOSFET gate to source voltage
t_{on}	Turn on time
t_{off}	Turn off time
f_s	Switching frequency
R_s	Stator resistance
$R_{DS(on)}$	MOSFET on state resistance
I_{sense}	Measured phase current
Q_{Gtot}	Total gate charge
V_{Cdrop}	Capacitor voltage drop
V_γ	Diode forward voltage
f_{sw}	Switching frequency
eff	Efficiency
P_{OUT}	Output power
P_{IN}	Input power
P_{loss}	Power loss
$T_{junction}$	Junction temperature
T_{amb}	Ambient temperature
$R_{\theta j-a}$	Junction to air thermal resistance
$R_{\theta j-c}$	Junction to case thermal resistance
$R_{\theta(c-a)}$	Case to air thermal resistance
L_d	Direct inductance
L_q	Quadrature inductance
P_C	Conduction losses
P_S	Switching losses

P_L	Leakage losses
i_d	Drain current
C_{iss}	Input capacitance
t_{ri}	Current rise time
t_{fi}	Current fall time
t_{rv}	Voltage rise time
t_{fi}	Voltage Fall time
J	Inertia
α	Angular acceleration
B_f	Friction coefficient
ω_n	Natural angular frequency
θ	Angle
ζ	Damping ratio

Abbreviations

ADC	Analog-to-Digital Converter
BJT	Bipolar Junction Transistor
BLDC	Permanent Magnet Synchronous Machine
CAD	Computer Aided Design
CAN	Controller Area Network
CFD	Computational Fluid Dynamics
DTC	Direct Torque Control
EMF	Electromotive Force
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FEM	Finite Element Method
FOC	Field Oriented Control
HRPWM	High Resolution Pulse Width Modulation
IGBT	Insulated-Gate Bipolar Transistor
ISR	Interrupt Service Routine
MCU	Micro-Controller Unit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor

PCB	Printed Circuit Board
PI	Proportional Integral
PMSM	Permanent Magnet Synchronous Machine
PWM	Pulse Width Modulation
RLC	Resistor, Inductor, Capacitor circuit
RM-IPM	Interior Permanent Magnets with Radial Magnetization
SOC	Start Of Conversion
TIM	Thermal Interface Material
TM-IPM	Interior Permanent Magnets with Tangential Magnetization
VSD	Variable Speed Drive

Chapter 1

Introduction

1.1 Background

Since the advent of the synchronous machine in the late 19th-century, [5] it has become one of the most important electromechanical devices in modern society. The synchronous machine plays a vital role in our ability to produce the ever-growing need for electrical power. However, with the growing need for renewable and green energy, the efficiency of synchronous machines has become the key focus in many industries. This has led to the discovery and development of using permanent magnets in synchronous machines. The use of permanent magnets allows for a higher efficiency as well as better power to weight ratios with the compromise of added cost. As a result of this, they are ideally suited for low to medium power applications, such as wind turbines and lightweight vehicles.

In many permanent magnet synchronous machine (PMSM) applications, the machine is supplied by or supplying a DC source thus, additional control hardware is required. This hardware can play a very large role in the total efficiency of the machine system. These losses can be due to multiple factors such as the different control schemes used, or the choice of switches within the inverter. Additionally the overall efficiency of the system can often be improved if the control hardware can be configured specifically for the machine and its application.

Over the last decade, simulation has become the key element in mitigating disadvantages in all areas of electronics. This is as a result of the dramatic increase in computing power, following Moore's law. Thus, making it possible for engineers to test multiple variations of a design at very little cost. Thus, they are able to tailor designs to applications, reducing compromises without the need to do as much costly physical testing.

1.2 Project motivation

1.2.1 Problem statement

The ideal design for a PMSM drive is one that is capable of supplying the exact maximum currents required by the machine, resulting in the least possible losses, at the lowest possible cost. Additionally, the design must have the smallest, most cost-effective and most practical cooling solution whilst maintaining reliability.

This project aims is to develop a method in designing a PMSM drive to increase the probability of a successful single revision design, whilst also achieving a number of secondary aims. These secondary aims are to increase the overall design reliability and optimise overall

power density.

To achieve this the focus of the methodology is placed on identifying design vulnerabilities and areas for optimisation during the design process. This allows these areas to be addressed before production, resulting in a single revision design with a high reliability and the best possible power density.

As discussed in further detail in section 4.2.2 temperature is the largest contributing factor of stress to electronic devices. This combined with semiconductors and PCB's being the most common root causes for failure [6], the inverter stage of the variable speed drive (VSD) is the key focus point for the design methodology.

1.2.2 Project objectives

To successfully achieve the aim of this project of developing and testing a VSD design methodology with the use of an example, the following objectives must be met.

The first objective which must be met is the successful simulation of the PMSM drive. This simulation must use a three-phase inverter with ideal switches. From this simulation, it will be possible to determine the maximum current and voltage, per switch within the inverter. Knowing this a set of switch specifications can be compiled, allowing a selection of switches to be made.

A second simulation must be developed to allow the testing of each of the switches in the selection. The testing must be able to determine the total switching and conduction losses within the three-phase inverter, for any switching frequency. This allows for a comparison to be made between different switching frequencies aiding in the compromise between switching losses and current ripple.

The final simulation objective in this project is to use computational fluid-dynamics and thermodynamics software (CFD) for design optimisation and analysis. Methods in which to improve the component layout of the three-phase inverter must be identified. This is done to aid in maintaining a uniform temperature between all switches. Using the total losses attained in previous simulations each switch option must then be simulated to determine the maximum temperature reached within the three-phase inverter.

Using the results from these simulations the optimal switch must be chosen, after which the final design of a 5 kW PMSM drive must be completed. This design must then be simulated to determine its thermal resistance, allowing sufficient cooling designs to be fabricated by the end user.

Finally, the completed design example must be operated with a known losses value allowing for the verification of the thermal simulations.

Chapter 2

Variable speed drive design methodology overview

2.1 Introduction

In this chapter a detailed overview of the methodology developed for the design of a variable speed drive is discussed.

The chapter begins with a flow diagram of the design methodology after which each block is discussed in detail.

2.2 Design methodology

2.2.1 Section overview

The design methodology discussed below in Figure 2.1 and further in sections 2.2.2 to 2.2.10 follows the principle of the modular design method presented in (Dong Jiang et al., 2018), which is based on the concept of "power electronics building blocks (PEBB)". By following this method, the design methodology is split between two modules, these being the high current inverter module and the low current control module. This method of modular design allows for a reduction in the complexity of the over all simulation process which is further discussed in section 4.2.3.

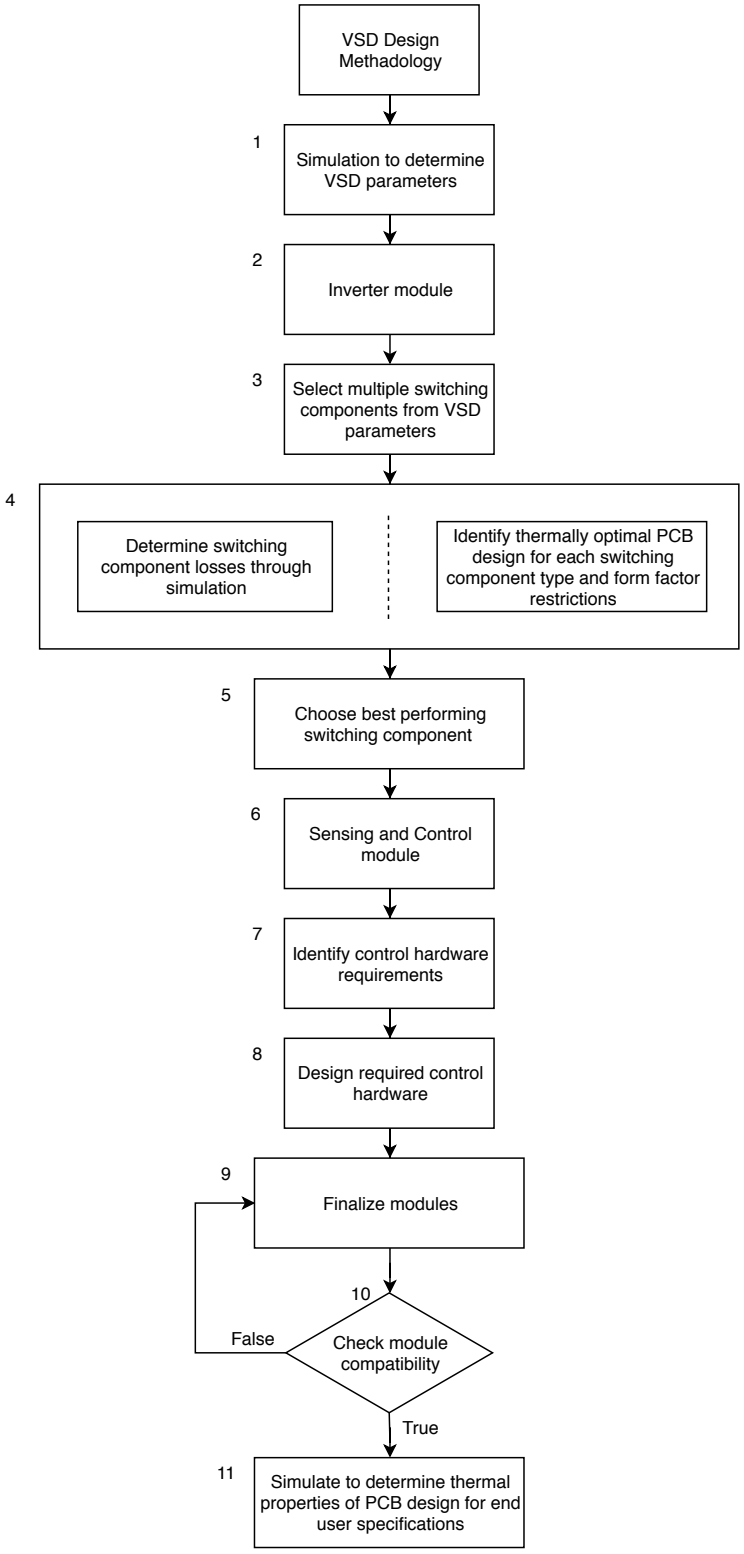


Figure 2.1: Design methodology flow diagram.

2.2.2 Simulation to determine VSD parameters

In this stage of the design methodology the aim is to determine the operating conditions at which the major components within the VSD are expected to operate. Knowing these operating conditions, a set of specifications for the components within the VSD can be formulated. This process is achieved by using Matlab Simulink and can be seen in more detail in section 3.3.

2.2.3 Selecting switching components

During this stage of the design methodology a selection of switching components are chosen to allow for a comparison to be performed between them as seen in section 3.4.

The switching components are focused on due to their large contribution of the VSD losses which are present in the form of heat. This is of great importance as heat is one of the largest contributing factors to the reliability of electronic equipment as discussed in section 4.2.2.

2.2.4 Determining switching losses

The first step in determining the switching losses for each MOSFET option is to implement them in the Simulink simulation. The method used to achieve this is discussed in more detail in section 3.6.2.

After the implementation of the MOSFETs has been completed the switching losses must be simulated. Due to an inaccurate method used to determine the switching voltages and currents in Simulink, a method discussed in section 3.6.3 is used. As a consequence of the use of this method the total simulation time is also reduced due to the increase in the maximum simulation step size. Finally the conduction losses are simulated and added to the switching losses attaining the total losses.

2.2.5 Thermally optimal PCB designs

As a result of the different device properties of each of the switching component options, the PCB configuration for each component may be required to be different. For this reason, in this stage of the design methodology each PCB configuration is simulated to purely optimise the heat distribution throughout the PCB design. To achieve this, a sufficiently accurate simple thermal model of the switching component package must be created. This is discussed in section 4.4 after which the PCB thermal optimisation process is discussed in section 4.5.

2.2.6 Selection of best performing switching component

In this stage of the design methodology the aim is to select the best switching component. This is achieved by comparing the simulated losses, simulated temperature, cost and possible design complexities which can be seen in section 4.6.

2.2.7 Identification of sensing and control hardware

The aim of this stage in the design methodology is to use the simulations to identify all the control hardware required, as well as the sensing circuitry needed for this hardware to operate.

2.2.8 Design and finalization of hardware

At this stage of the design process all the hardware decisions should be made, and each hardware module design completed with the others in mind.

2.2.9 Module compatibility

Due to the nature of modular design, it is critical to ensure the complete compatibility between modules. If the designs are not compatible the design should enter back into the previous stage of the the methodology. It is however possible that substantial changes may need to be made, in which it is then required to enter back into a previous simulation stage of the methodology. An example of such changes is a change in switching component package type or substantial PCB form factor changes.

2.2.10 Specifications for end user

This is the final stage of the design methodology and process which is in fact completed after the design has been finalised. This stage is comprised of performing any simulations or calculations to provide the end user with sufficient product specifications to allow the safe and reliable use of the VSD.

2.3 Chapter summary

In the chapters to follow this design methodology is further explained and tested through the use of example. The example chosen is to design and build a 5 kW drive for the PMSM used in the Mellowcabs vehicle. It is important to note however, that this methodology can be used in the design of a VSD of ranging output power as well as for applications not only including the PMSM. Additionally, with little alteration this methodology can also be used in the development of many power electronics applications such as single phase inverters and DC-DC switching converters.

Chapter 3

Simulation of an inverter for a PMSM

3.1 Introduction

This chapter covers the Matlab simulations of a three-phase inverter to drive a PMSM. The aim of these simulations is to determine the currents through the switches as well as the total losses within them. This also allows for a selection of different switches to be tested identifying which would be the most efficient option.

The chapter begins with a brief overview of permanent magnet machines and their control schemes. Transistors are then discussed primarily focusing on IGBT's and MOSFET's. Following this the Matlab simulation is then discussed, where the focus is placed on the MOSFET bridge as well as the measurement of total power and losses.

3.2 Literature related to 3 phase inverters for PMSM

3.2.1 Literature overview

In order to simulate the currents within a PMSM based three-phase inverter, a basic understanding of a PMSM is required. Thus, a short study was done on permanent magnet machines.

When designing a three-phase inverter, choosing the correct switching components is often the most important design decision. Thus, a short study is done into the types of semiconductor switches and their operation. From this study, it can be seen that the MOSFET is the ideal semiconductor switch to be used in a low voltage 5 kW inverter. One of the key reasons for this is the ability to place MOSFETs in parallel which is further investigated. Due to the primary objective of this chapter being to simulate the total losses within a three-phase inverter. An investigation is done into calculating the total losses within a MOSFET.

3.2.2 Brushless motors

The simplest form of an electrical motor is the brushed DC motor. However, brushed DC motors tend to have low reliability. This is due to the wear caused by physical contact between the brushes and the commutators. Brushless motors do not have this reliability problem but do require more complex control. Nevertheless, this complex control can be a benefit in many applications. Some of these benefits include more accurate rotational velocity, smoother torque output and in some cases exact angular control.

From Figure 3.1 it can be seen that there are two classes of brushless motors, these being DC and AC.

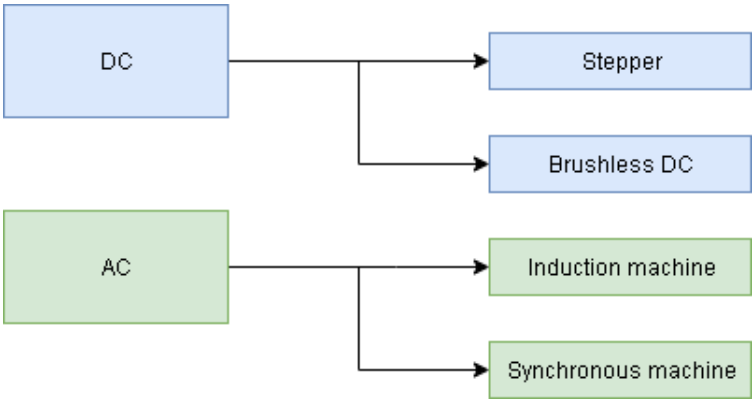


Figure 3.1: Types of brushless motors.

The stepper motor is an example of an application in which there is the benefit of exact angular control. These are used in applications such as printers where discreet movement is needed. Stepper motors are controlled by applying a sequence of alternating DC pulses to the coils.

Induction motors are simple in design and construction, which aids in their high robustness and reliability while maintaining a low cost. There are two main types of induction motors with the differentiating factor being the rotor winding type. The most common type is the squirrel cage configuration in which solid copper bars are placed within the rotor at a slight angle. These bars are then joined at each end which allows for a current loop. The less common configuration is the wound rotor which contains three-phase windings similar to that of the stator. The reason this option is less common is due to the need for slip rings which increases the maintenance requirements.

Induction machines are also ideally suited for applications where very high rotational speeds are needed. Typically if the surface speed of the rotor is greater than 250 m/s an induction motor is better suited due to the centrifugal forces on the rotor.

Although induction machines have many benefits, permanent magnet machines are becoming more popular due to their higher efficiency and power to weight ratio which can be achieved.

Permanent magnet machine rotors typically have one of the three structures seen in Figure 3.2 [7]. These structures determine the back-EMF waveforms and thus, how the machine should ideally be controlled. It can also be seen that for the RM-IPM and TM-IPM structures the magnets are placed within the rotor. This greatly increases the maximum rotational speed that can be achieved as the magnets do not risk breaking off the rotor. Additionally, due to the magnetization of the rotor, the structure has an effect on the relationship between the direct and quadrature inductance values. Typically for rotors with surface mount magnets $L_d \approx L_q$, whereas for rotors with interior magnets with radial magnetization $L_d \approx 0.5 \times L_q$ [8–10].

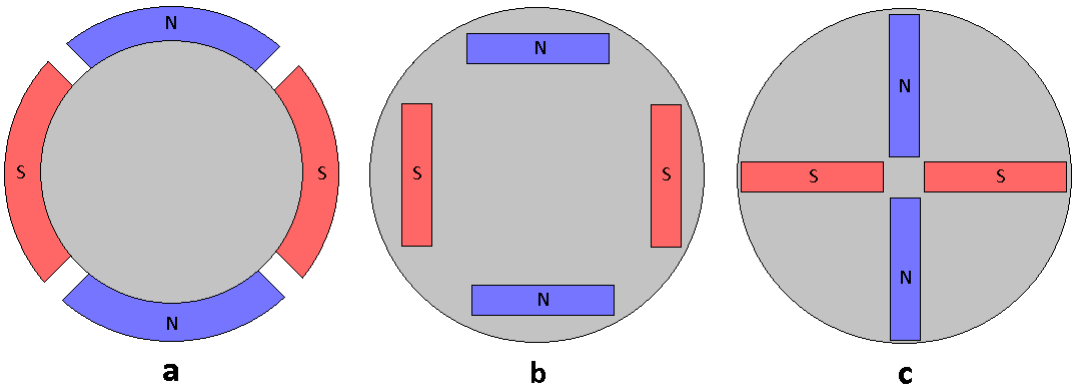
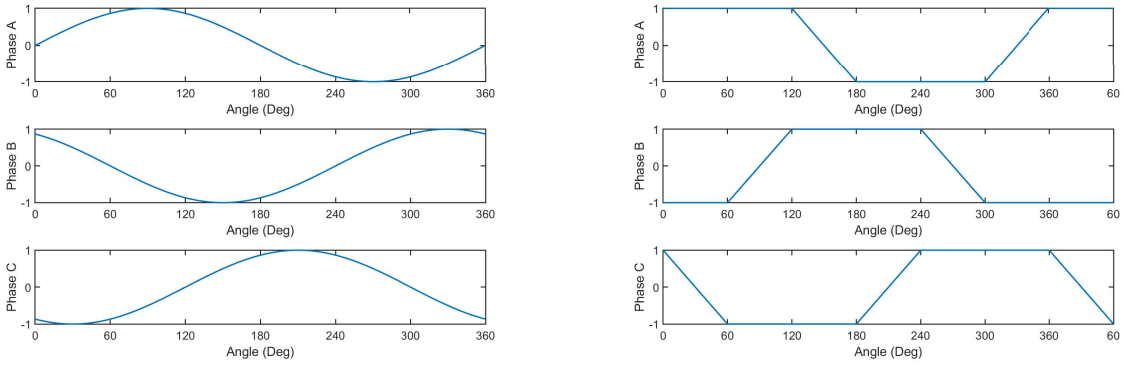


Figure 3.2: Rotor Structures: (a) Surface mount (SPM); (b) Interior magnets with radial magnetization (RM-IPM); (c) Interior magnets with tangential magnetization (TM-IPM).

The key characteristic of a brushless DC motor (BLDC) versus a PMSM is the back-EMF waveform and stator currents. The back-EMF for a BLDC machine follows that of a trapezoidal shape such as seen in Figure 3.3b [11] whereas for a PMSM the back-EMF is sinusoidal as seen in Figure 3.3a.



(a) PMSM back-EMF.

(b) BLDC back-EMF.

Figure 3.3: Back-EMF voltage profiles.

3.2.3 PMSM control

There are several control techniques that have been developed to drive a PMSM, some of which can be seen in Figure 3.4. These control techniques tend to be a compromise between simplicity, efficiency or reducing torque ripple.

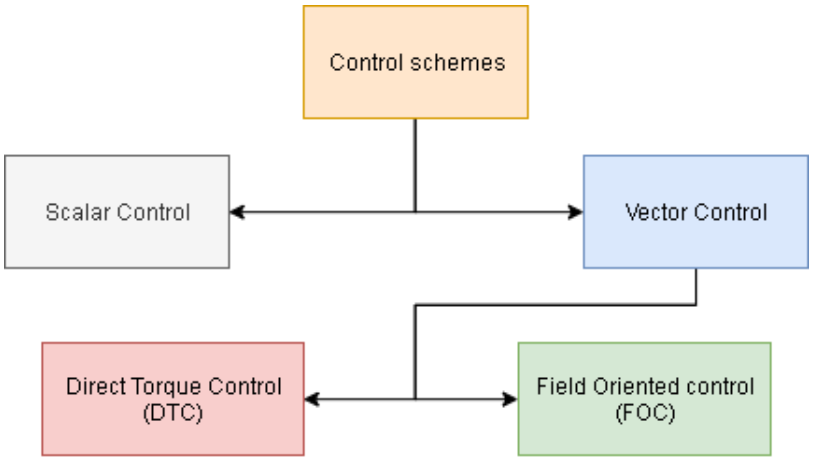


Figure 3.4: Types of PMSM control schemes.

3.2.3.1 Scalar control

Scalar control is the simplest method of controlling a synchronous machine, in which the ratio between voltages and currents are kept constant throughout the speed range. For a variation in the machine's speed to take place the output frequency is adjusted and therefore, due to the speed being directly related to the output frequency, the angle of the rotor is not needed. This lack of rotor angle sensor allows the total cost and complexity of the system to be reduced. However, by not having an angle sensor it makes the control system open loop and thus, the torque response is compromised [12].

3.2.3.2 Direct torque control

Direct torque control (DTC) which was introduced in the 1980s, directly controls the inverter states based on the PMSM's torque and flux values. This is done by finding the error between reference values and the measured torque and flux. If the error falls outside of a set hysteresis band the inverter is then set to another one of six predetermined states.

The implementation of direct torque control allows for a very robust system due to the low number of calculations required and the use of a lookup table. These characteristics also allow DTC to have a very low complexity while maintaining a good dynamic torque response [13]. However, DTC like scalar control does have the drawback of a relatively large torque ripple. Therefore, these control schemes are ideally suited for most industrial applications such as conveyor belts but not for sensitive applications such as hard drives.

3.2.3.3 Field oriented control

Field oriented control or flux oriented control is generally implemented to achieve better dynamic performance of a PMSM [14]. These improvements can be seen in the torque output at low speeds, a wider speed range due to field weakening and an overall improvement in efficiency [15]. FOC does, however, require multiple complex calculations such as the Park and Clarke transforms. Nonetheless, due to the advances in micro-controller speeds, the complex calculations can be completed within a very short time period.

The fundamental principle behind FOC is to keep the flux produced by the rotor orthogonal to the stator field, providing the maximum possible torque [16]. By using FOC it allows the decoupling of the flux and torque producing currents, thus allowing independent control of both [17, 18].

The principle of FOC requires three frames of reference, of which each is needed to calculate the next. The first frame of reference which can be seen in Figure 3.5 is the stator reference frame, of which each phase's currents (I_a, I_b, I_c) are normalised and 120° out of phase.

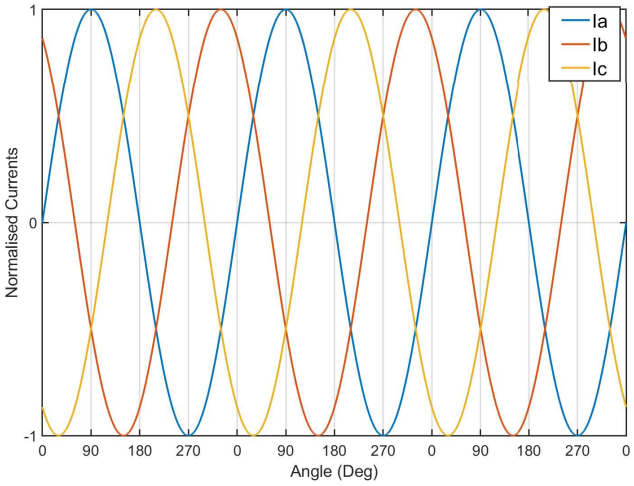


Figure 3.5: Stator reference frame.

The second frame of reference seen in Figure 3.6 is the orthogonal reference frame. This is calculated by using

$$I_\alpha = Ia; \quad I_\beta = \frac{I_a + 2I_b}{\sqrt{3}}, \tag{3.1}$$

which is known as the Clarke transform. The orthogonal reference frame is in the same plane as the stator reference frame, however, the transformed currents I_α and I_β are 90° out of phase.

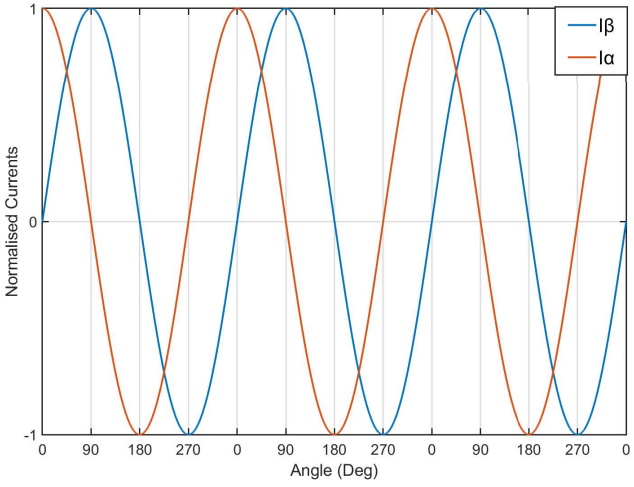


Figure 3.6: Two-phase reference frame.

The third frame of reference seen in Figure 3.7 is the rotor reference frame, in which the direct and quadrature axes currents are represented. This is calculated by using the Park

transform which can be seen as

$$I_d = I_\alpha cos(\theta) + I_\beta sin(\theta); \quad I_q = I_\beta cos(\theta) - I_\alpha sin(\theta), \tag{3.2}$$

where I_d is the direct axis current and I_q is the quadrature axis current. The direct axis is aligned along the North and South poles of the PMSM whereas the quadrature axis is 90° out of phase from the direct axis.

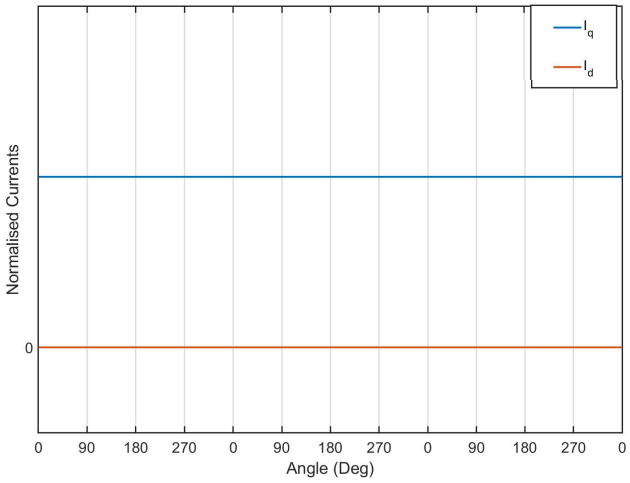


Figure 3.7: Rotating reference frame.

A PI control system is then implemented as seen in Figure 3.8 to calculate the desired V_d and V_q values. This is done to correct the error between the above-calculated values and the desired reference values.

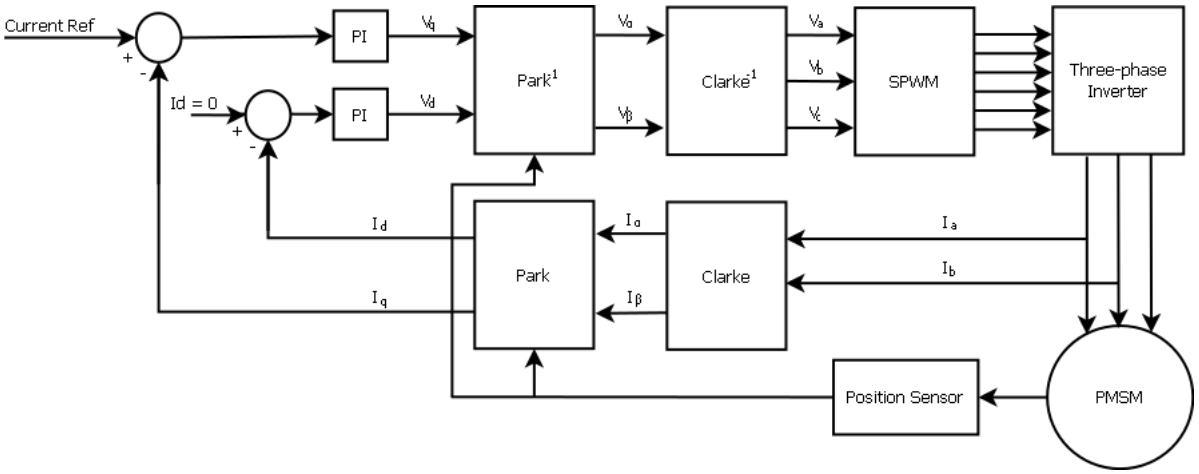


Figure 3.8: PI control system for FOC.

As seen in Figure 3.8, after the PI control system has calculated the desired V_d and V_q values, the inverse Park transform of

$$V_\alpha = V_d cos(\theta) - V_q sin(\theta); \quad V_\beta = V_q cos(\theta) + V_d sin(\theta) \tag{3.3}$$

is implemented. To calculate the desired normalised output voltage of V_a, V_b and V_c the inverse Clarke transform of

$$V_a = V_\alpha; \quad V_b = \frac{-V_\alpha + \sqrt{3}V_\beta}{2}; \quad V_c = \frac{-V_\alpha - \sqrt{3}V_\beta}{2}, \tag{3.4}$$

must be used.

3.2.4 MOSFETs and IGBT comparison

Due to its high current handling capabilities, the BJT used to be the only viable power semiconductor. This was up until the introduction of the MOSFET in the 1970's [19]. The BJT requires high base currents, has a relatively slow turn off characteristics and a negative temperature coefficient [20]. The MOSFET is a voltage-controlled device, thus having very low gate currents and has a positive temperature coefficient. However, the thin oxide layer of the MOSFET is very sensitive to overvoltages and thus, special consideration needs to take place in high voltage designs. The IGBT combines the voltage-controlled properties of a MOSFET with the high current capabilities of a BJT however, the slow turn off time as well as the negative temperature coefficient remain.

The two forms of semiconductor switches which are ideally suited for the application of a 5 kW three-phase inverter, are the MOSFET and IGBT. However, due to the properties of the MOSFET and IGBT, it can be identified that MOSFETs are well suited for low to medium voltages or high-frequency switching applications [1]. Figure 3.9 below shows voltage vs frequency and indicates the ideal application for each device. From this investigation, it is clear that MOSFETs are the fitting choice for a 24-48 V 5 kW three-phase inverter.

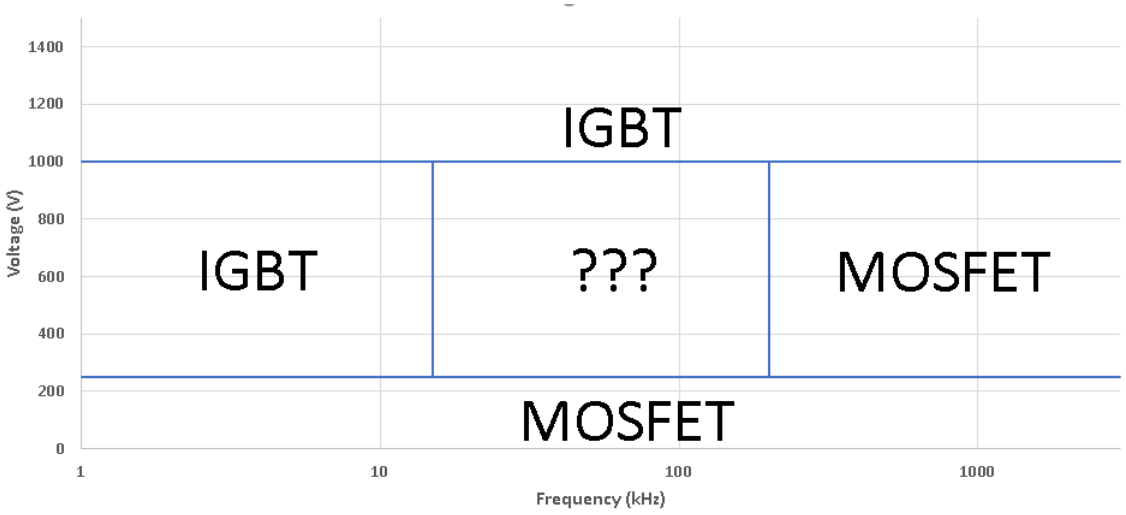


Figure 3.9: MOSFET vs IGBT applications [1].

3.2.5 Losses within MOSFETs

Power losses due to MOSFETs used in switching applications are broken into three areas known as conduction (P_C), switching (P_S) and leakage (P_L) losses. The leakage losses are typically very small and thus, are neglected in this design methodology [21].

3.2.5.1 Conduction losses

When a MOSFET is being used in a switching application it is represented as an open circuit or a resistor known as R_{DSon}. To calculate the instantaneous conduction losses in a

MOSFET

$$p_C(t) = v_{DS}(t) \times i_D(t) = R_{DSon} \times i_D^2(t) \tag{3.5}$$

is used, where v_{DS} is the drain to source voltage and i_D is the drain current [21].
By integrating the instantaneous conduction losses over a switching period with

$$P_C = \frac{1}{T} \cdot \int_0^T R_{DSon} \cdot I_D^2(t)dt, \tag{3.6}$$

the average conduction losses can be calculated.

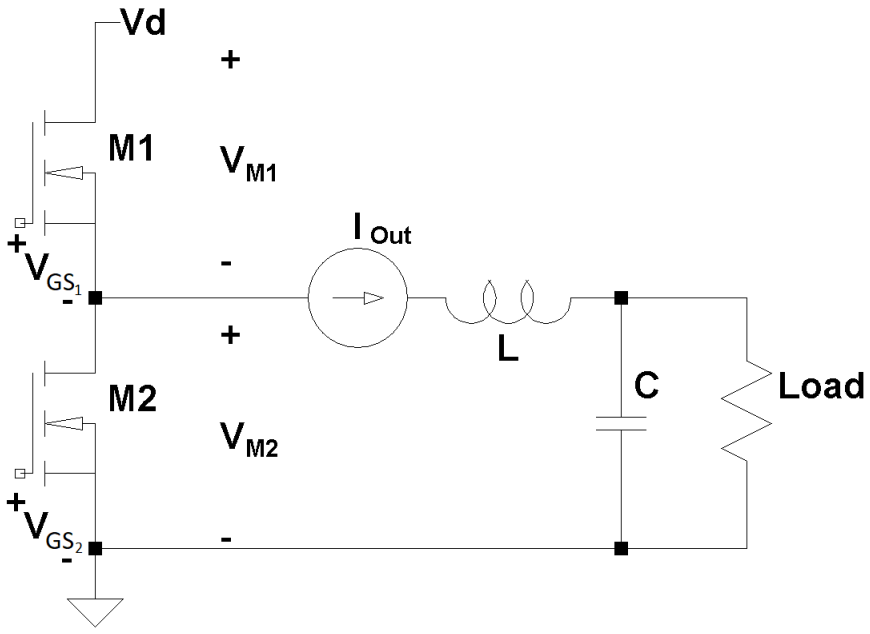


Figure 3.10: Simple buck converter circuit.

A simple buck converter can be seen in Figure 3.10, where it will be assumed that ripple on the output voltage and current is negligible. This is used, as a three-phase PMSM drive is in essence, three buck converters with a sinusoidal output current. Due to the operation of a buck converter, the $i_D(t)$ and $v_{DS}(t)$ of the MOSFETs $M1$ and $M2$ can be described by

$$\begin{aligned} For\ M1 &: \begin{cases} 0 < t < D & i_D = I_{Out}; \quad v_{DS} = I_{Out} \times R_{DSon} \\ D < t < T & i_D = 0; \quad\ \ v_{DS} = V_d - (I_{Out} \times R_{DSon}) \end{cases} \\ For\ M2 &: \begin{cases} 0 < t < D & i_D = 0; \quad\ \ v_{DS} = V_d - (I_{Out} \times R_{DSon}) \\ D < t < T & i_D = -I_{Out}; \quad v_{DS} = -I_{Out} \times R_{DSon} \end{cases} \end{aligned}, \tag{3.7}$$

where D is the duty cycle and T is the switching period.
From this, the total conduction losses can be calculated using

$$P_C = \frac{1}{T} \cdot \left[\int_0^D R_{DSon} \cdot I_{Out}^2 dt + \int_D^T R_{DSon} \cdot (-I_{Out})^2 dt \right]$$

$$P_C = \frac{1}{T} \cdot R_{DSon} \cdot I_{Out}^2. \tag{3.8}$$

3.2.5.2 Switching losses

For a MOSFET to turn-on, the gate to source voltage (V_{gs}) must be greater than the turn-on voltage (V_{TN}) of that specific MOSFET. A simple MOSFET model in Figure 3.11 shows that there are multiple RLC circuits. These RLC circuits have an effect on the rate at which V_{gs} can rise above V_{TN}. Additionally, V_{gs} is held constant for a time period due to the Miller effect. During this time is when the voltage across the MOSFET drops. This is what determines the time properties of MOSFETs in switching applications known as turn-on delay ($t_{On(Delay)}$), turn-on (t_{On}), turn-off delay $t_{Off(Delay)}$ and turn-off t_{off} times.

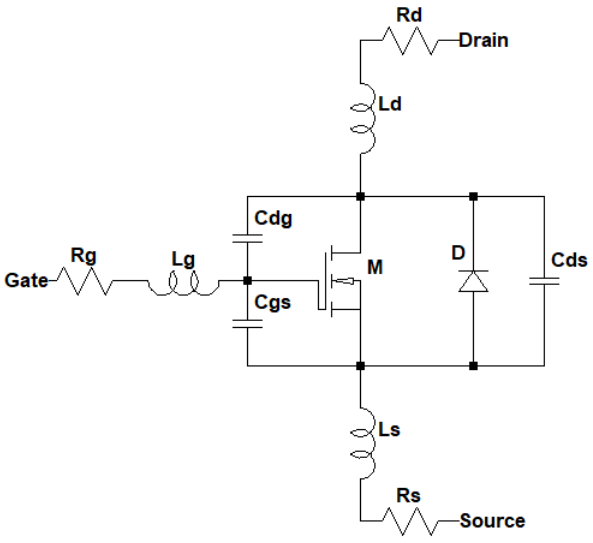
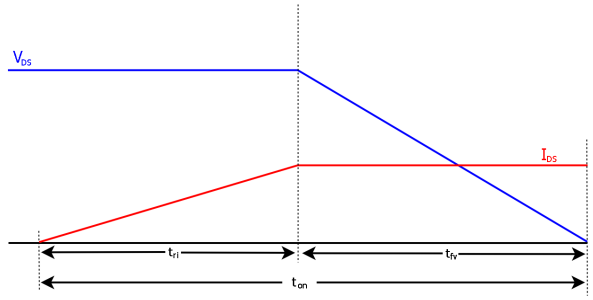
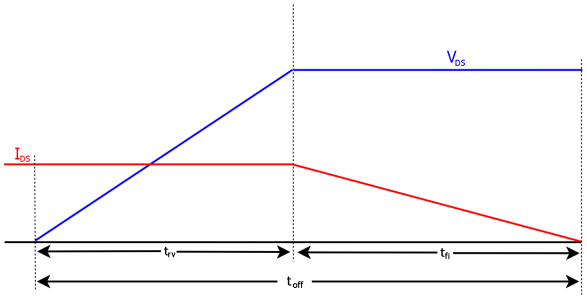


Figure 3.11: Basic MOSFET model [2].

During the turn-on time, the voltage across the MOSFET $M1$ (V_{M1}) in Figure 3.10 will be equal to $V_d - V_{M2}$. The current through $M1$ (I_{M1_D}) however will increase linearly from zero to I_{Out}. Once the current through the switch reaches the value of I_{Out} the voltage V_{M1} linearly decreases until it reaches $R_{DSon} \times I_{Out}$. This can be seen in Figure 3.12a. During the turn off time the current through the MOSFET will remain equal to I_{Out} while V_{M1} linearly increases again to a value of $V_d - V_{M2}$. After this the current will drop to zero again as seen in Figure 3.12b [22].



(a) For transition from off to on.



(b) For transition from off to on.

Figure 3.12: Voltage and current across switch.

By integrating the product of the voltage and currents for both the turn-on and turn off periods, the power lost in one switching cycle can be calculated. Thus,

$$P_S = \frac{1}{T} \cdot \left[\int_0^{t_{on}} v_{M1}(t) \cdot i_{M1}(t) dt + \int_0^{t_{off}} v_{M1}(t) \cdot i_{M1}(t) dt \right] \tag{3.9}$$

is used to calculate the total average switching losses within that switch, where T is the switching period.

Before the current in Figure 3.12a can begin rising, V_{gs} must rise above the MOSFET threshold voltage. The time it takes for V_{gs} to rise above V_{TN} is what determines the turn-on delay time of the MOSFET. To determine this as well as t_{ri}, t_{fv}, t_{rv} and t_{fi}, the MOSFET gate circuit model in Figure 3.13 is used.

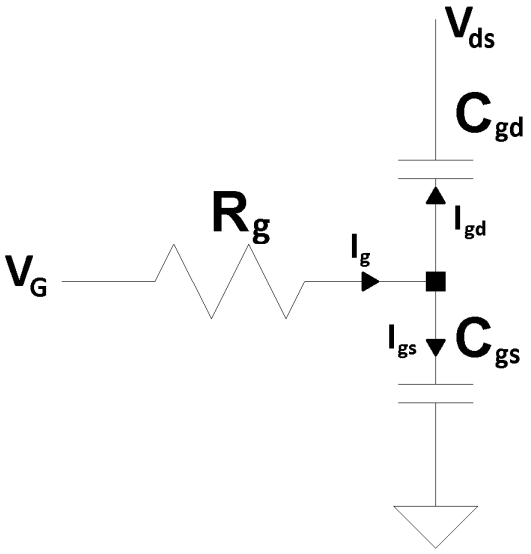


Figure 3.13: MOSFET gate circuit.

To determine the times mentioned above the gate current is needed, thus

$$I_g = \frac{V_G - V_{gs}}{R_g} \tag{3.10}$$

$$I_g = I_{gs} + I_{gd}. \tag{3.11}$$

I_{gs} and I_{gd} can be represented as

$$I_{gs} = C_{gs} \cdot \frac{dV_{gs}}{dt} \tag{3.12}$$

$$I_{gd} = C_{gd} \cdot \frac{d(V_{gs} - V_{DS})}{dt}, \tag{3.13}$$

where due to V_{DS} being constant

$$I_{gd} = C_{gd} \cdot \frac{d(V_{gs})}{dt}. \tag{3.14}$$

Thus,

$$I_g = C_{gs} \cdot \frac{d(V_{gs})}{dt} + C_{gd} \cdot \frac{d(V_{gs})}{dt}$$

$$= (C_{gs} + C_{gd}) \cdot \frac{d(V_{gs})}{dt}, \tag{3.15}$$

which can be rearranged to

$$\frac{dV_{gs}}{V_G - V_{gs}} = \frac{dt}{R_g \cdot (C_{gs} + C_{gd})}. \tag{3.16}$$

(3.16) is then integrated to

$$-ln(V_g - V_{gs}) = \frac{t}{R_g \times (C_{gs} + C_{gd}} + k, \tag{3.17}$$

where to solve for constant k, (3.17) is then rearranged to

$$V_{gs} = V_G - k \times e^{\frac{-t}{R_g \times (C_{gs} + C_{gd})}}, \tag{3.18}$$

allowing k to be solved for knowing that at $t = 0$, $V_G = 0$ and $V_{gs} = 0$, thus

$$V_{gs} = V_G \left(1 - e^{\frac{-t}{R_g \times (C_{gs} + C_{gd})}}\right). \tag{3.19}$$

To simplify the above equations the variable C_{iss} is introduced as the input capacitance seen by the gate driver which can be described by

$$C_{iss} = C_{gs} + C_{gd}. \tag{3.20}$$

This allows (3.19) to be simplified to

$$e^{\frac{-t}{R_g C_{iss}}} = 1 - \frac{V_{gs}}{V_G}, \tag{3.21}$$

after which it is then manipulated to

$$t = R_G C_{iss} \times ln\left(\frac{1}{1 - \frac{V_{gs}}{V_G}}\right). \tag{3.22}$$

Using (3.22) all of the turn-on times can be found as

$$t_{OnDelay} = R_G C_{iss} \times ln\left(\frac{1}{1 - \frac{V_{TH}}{V_G}}\right), \tag{3.23}$$

$$t_{ri} = R_G C_{iss} \times ln\left(\frac{1}{1 - \frac{V_{gp}}{V_G}}\right) - t_{OnDelay}, \tag{3.24}$$

and

$$t_{fv} = R_G C_{gd} \frac{V_{DS}}{V_G - V_{gp}}. \tag{3.25}$$

Using the same principles for attaining the turn-on time equations, the turn off time equations were found as

$$t_{rv} = R_G C_{gd} \frac{V_{DS}}{V_{gp}} \tag{3.26}$$

and

$$t_{fi} = R_G C_{iss} \times ln\left(\frac{V_{gp}}{V_{TH}}\right). \tag{3.27}$$

3.2.6 MOSFETs in parallel

One of the benefits of MOSFETs is that due to their structure they can easily be placed in parallel which can be very beneficial in situations where controlling high currents is needed. Part of the reason why MOSFETs can be placed in parallel is due to their negative temperature coefficient. As one MOSFET in a group carries a slightly higher current than the others its temperature increases. This in turn, increases its R_{DSon} decreasing its conductivity and thus, the others in the group conduct more. This is a form of self-balancing that is permanently taking place between the MOSFETs in parallel until they reach an equilibrium. However, there are several potential problems that can occur when placing MOSFETs in parallel. Therefore, the following considerations should be carefully taken during the design process.

As mentioned above the negative temperature coefficient of the MOSFET allows it to form a stable current equilibrium when placed in parallel with other MOSFETs. This does however only apply if the junction to air thermal resistance ($R_{\theta(j-a)}$) of each MOSFET is exactly the same. Therefore, it is vitally important that the PCB layout is optimised to best keep the case to air thermal resistance ($R_{\theta(c-a)}$) identical for each MOSFET. Additionally, the junction to case ($R_{\theta(j-c)}$) thermal resistance of each MOSFET may differ and cannot be controlled. Thus, even if the $R_{\theta(c-a)}$ can be made exactly identical for each MOSFET their $R_{\theta(j-a)}$ will differ due to the production process which can cause an imbalance in currents. Due to this, there must be a safety factor added to the maximum current per MOSFET when choosing a device.

As mentioned in section 3.2.5.2 the gate resistance and inductance have an effect on the turn-on time of the MOSFET. If the turn-on times for each MOSFET in parallel differ substantially the turn-on currents of the fastest MOSFET may greatly exceed the maximum capabilities of the device. Thus, it is vital in the design to keep all traces between the MOSFET driver and each MOSFET short or of equal lengths. Additionally, it is good practice to place a resistor at the gate of each MOSFET as seen in Figure 3.14. This has the effect of making the difference in gate resistances negligible, thus resulting in a fairly uniform turn-on time between components. However, adding a gate resistor has the negative effect of slowing down the turn-on time which leads to greater switching losses. Therefore, careful consideration must be taken in choosing this resistor value.

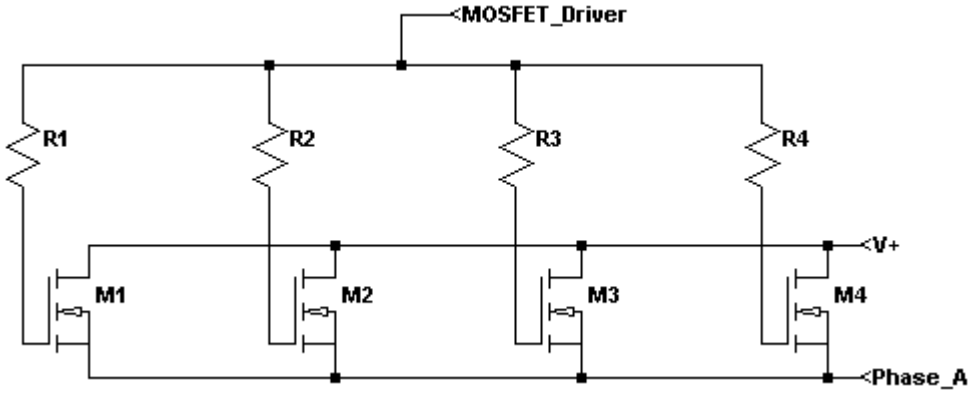


Figure 3.14: Individual gate resistors for uniform turn-on time.

3.3 Simulation to determine VSD parameters

3.3.1 Section overview

The primary aim of simulating the three-phase PMSM drive in this section is to determine the currents through the three-phase inverter. This is done to determine a set of minimum requirements for choosing components. Additionally, the simulation is also required to be structured in a manner that allows for multiple different MOSFET options to be tested in section 3.6.

In Figure 3.15 an overview of the simulation model can be seen. Key sections are focused on in detail such as the simulation configuration to ensure realistic and as close to accurate results.

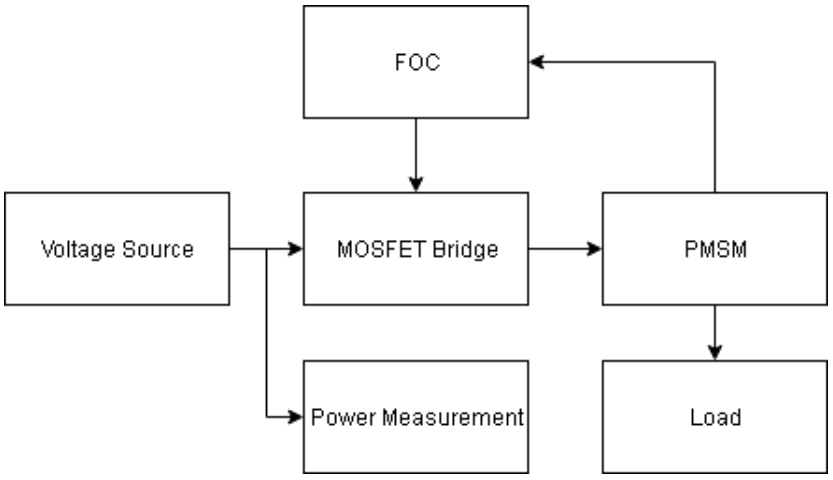


Figure 3.15: Simulation overview.

3.3.2 Three-phase MOSFET bridge

A three-phase MOSFET bridge designed for use with a balanced load is traditionally made up of six switches. Theses switches are placed in the topology as seen in Figure 3.16.

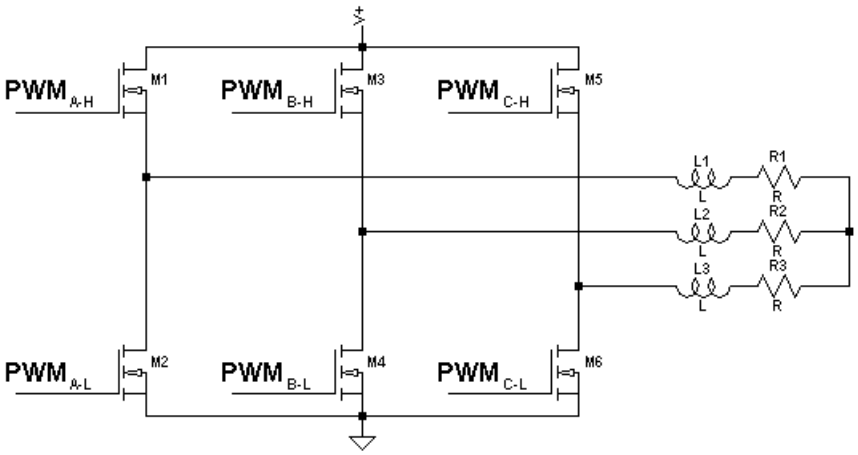


Figure 3.16: Three-phase MOSFET bridge.

The aim of the simulations in this section is focused purely on the voltages and currents experienced by the MOSFETs and thus, does not include losses. Due to this the MOSFETs

are configured to be as close to ideal switches as possible. To achieve this the gate capacitance's of the MOSFETs are set to 0 pF. This will cause the switching times to be calculated as zero seconds and thus, the switching losses will be zero watts. Additionally, the on-state resistance of the switches are also set to a very low value. This reduces the voltage drop over the MOSFETs to a negligible amount, resulting in close to zero conduction losses.

Figure 3.17 shows a small time period of the voltage and current through the low side switch on phase C. From this, it can be seen that the turn-on and off times, as well as the voltage drop due to the on-state resistance is negligible. Thus, the aim of simulating an ideal switch was achieved.

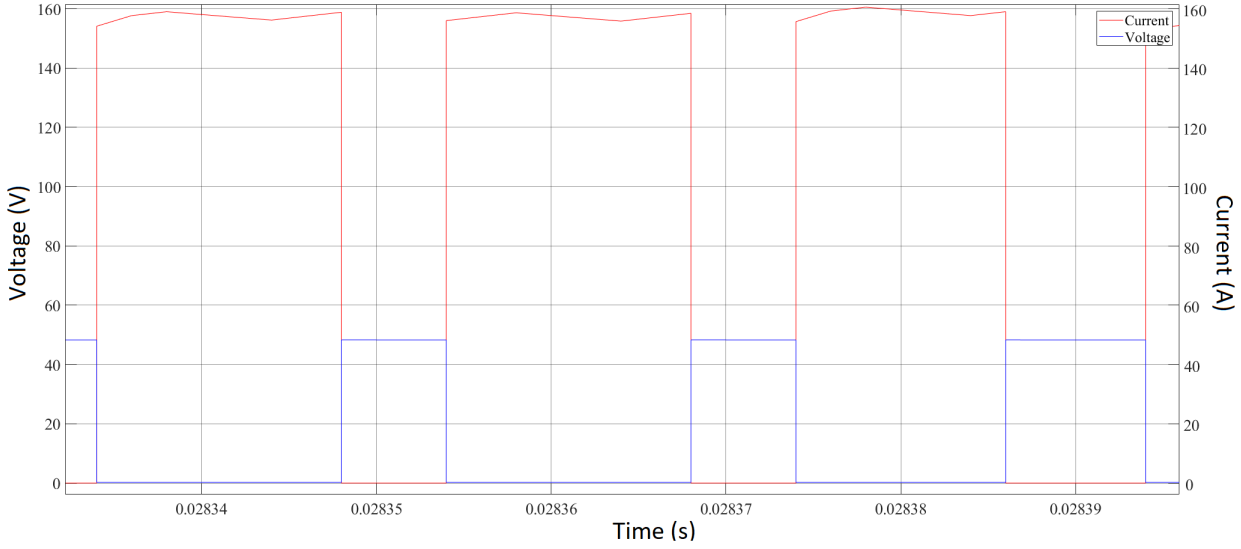


Figure 3.17: Voltage and current vs time.

3.3.3 PMSM parameters

Within Matlab Simulink, a PMSM is supplied in the Simscape power electronics package. This model can be seen in Figure 3.18 with terminals $\sim$, n, C and R.

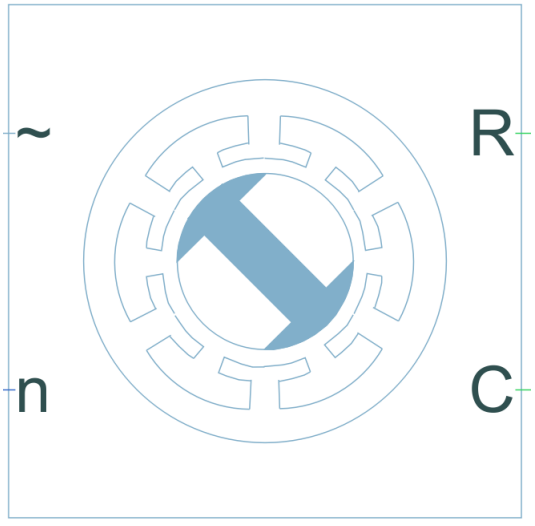


Figure 3.18: PMSM Matlab model.

To accurately simulate the PMSM a number of key parameters are required. The main parameters are the number of pole pairs, stator resistance (R_s), direct axis inductance (L_d) and quadrature axis inductance (L_q). To determine the pole pairs of a PMSM, a constant low current is applied through phases A and B. The rotor must then be rotated whilst taking notice of the number of positions at which the rotor settles. From this, the number of pole pairs within the machine can be determined. At the same time, the stator resistance can be calculated by utilising ohms law since the current through the two phases as well as the voltage over these phases is known. To improve the accuracy of this the average of four or more samples should be taken with varying current values. Due to the fact that the current used for measurement is DC whereas the current through the machine during operation will be AC, it is important to consider the skin effect. However, this was not taken into account in this example application due to the low fundamental frequency of the machine and the use of a combination of thin wires for the phase windings making the skin effect negligible.

To determine the synchronous inductances it is first required to determine the structure of the machine. For this reason as well as to determine the operation of the rotor angle sensor, the machine used in the example application was dismantled. It was observed that the machine contains interior magnets with radial magnetization as seen in Figure 3.19. From section 3.2.2 it is known that $L_d \approx 0.5 \times L_q$, therefore it is only necessary to measure the direct phase inductance.

Figure 3.19: Rotor shaft.

To measure the direct phase inductance the output of a signal generator is set to 20 kHz with a 1 V_{p-p} amplitude. The phase A and B terminals are then connected to the output of the signal generator. After connecting the PMSM to the signal generator the frequency is adjusted to achieve an output signal of 0.5 V_{p-p}. The phase inductance can then be calculated using

$$L = \frac{4.57}{f}, \tag{3.28}$$

where f is the frequency the signal generator was adjusted to.

(3.28) can be determined due to the relationship between the voltage of the oscilloscope and the signal generator which can be seen by

$$\left|\frac{V_{scope}}{V_{gen}}\right| = \left|\frac{j\omega L}{R+j\omega L}\right| = \left|\frac{j\omega L}{R+j\omega L}\cdot\frac{R-j\omega L}{R-j\omega L}\right| = \left|\frac{j\omega RL+\omega^2L^2}{R^2+\omega^2L^2}\right| =$$

$$\left|\frac{\omega^2L^2}{R^2+\omega^2L^2}+j\frac{\omega LR}{R^2+\omega^2L^2}\right| = \sqrt{\frac{\omega^4L^4}{(R^2+\omega^2L^2)^2}+\frac{\omega^2L^2R^2}{(R^2+\omega^2L^2)^2}} =$$

$$\frac{\sqrt{\omega^4L^4+\omega^2L^2R^2}}{R^2+\omega^2L^2} = \frac{\sqrt{\omega^2L^2(R^2+\omega^2L^2)}}{R^2+\omega^2L^2} = \frac{\omega L}{\sqrt{R^2+\omega^2L^2}}, \tag{3.29}$$

where R is the 50 Ω resistance of the signal generator and ω is the radial frequency. Therefore,

$$\left|\frac{V_{scope}}{V_{gen}}\right| = 0.5 \Rightarrow \frac{\omega L}{\sqrt{R^2+\omega^2L^2}} = 0.5,$$

which can be rearranged to

$$\frac{\omega^2L^2}{R^2+\omega^2L^2} = \frac{1}{4}$$

$$\therefore 4\omega^2L^2 = R^2+\omega^2L^2.$$

This allows L to be solved for by

$$L = \sqrt{\frac{R^2}{3\omega^2}} = \sqrt{\frac{1}{3}}\cdot\frac{R}{2\pi f} = \sqrt{\frac{1}{3}}\cdot\frac{50}{2\pi f}$$

$$\therefore L = \frac{4.57}{f}.$$

The PMSM model also includes two mechanical parameters that have to be determined. These parameters are the rotor inertia and the rotor damping coefficient. The parameters are determined using a pendulum attached to the rotor as seen in Figure 3.20.

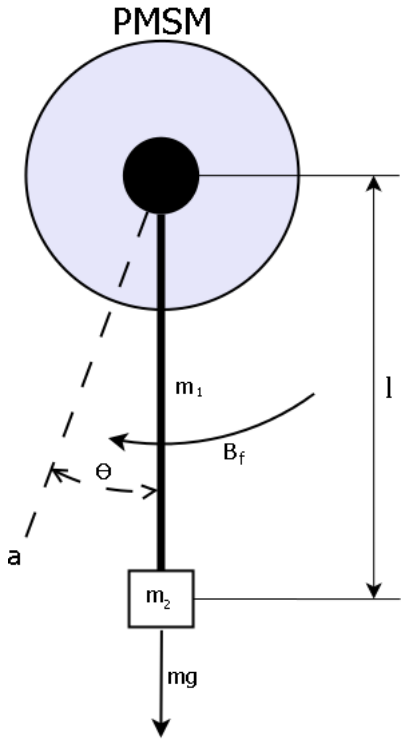


Figure 3.20: Pendulum attached to rotor.

With the pendulum added to the rotor, the total inertia is now made up of the individual inertias of, the pendulum J_1, the weight at the end of the rod J_2 and the rod J_3. However, due to m_1 being more than an order of magnitude less than the weight of m_2, the inertia of the rod is neglected. Therefore, the total inertia can be written as

$$J_{total} = J_1 + J_2 = J_1 + m_2 l^2. \tag{3.30}$$

Using Newton's law for rotational motion that is given by

$$M = J\alpha, \tag{3.31}$$

where M is the sum of the moments around the center of mass, J is inertia and α is angular acceleration. When the pendulum is at position a, it is then possible to represent the pendulum system as

$$(J_1 + m_2 l^2)\ddot{\theta} = -B_f\dot{\theta} - m_2 g l sin\theta, \tag{3.32}$$

where B_f is the friction coefficient and g is the gravitational acceleration constant of 9.81 m/s^2.

Using the Taylor series expansion, $sin(x)$ can be represented as

$$\begin{aligned} sin(x) &= \sum_{i=0}^{\infty} \frac{(-1)^i}{(2i+1)!} \cdot x^{2i+1} \\ &= x - \frac{x^3}{3!} + \frac{x^5}{5!} - \frac{x^7}{7!} + \frac{x^9}{9!} \ \dots\ , \end{aligned} \tag{3.33}$$

and thus for small values of x, $sin(x)$ can be approximated to x. From this, we can then simplify (3.32) to

$$(J_1 + m_2 l^2)\ddot{\theta} = -B_f\dot{\theta} - m_2 g l\theta. \tag{3.34}$$

Knowing the equation of

$$0 = \ddot{\theta} + 2\zeta\omega_n\dot{\theta} + \omega_n^2\theta, \tag{3.35}$$

where ω_n is the natural angular frequency and ζ is the damping ratio, it is then possible to rearrange (3.34) to

$$0 = \ddot{\theta} + \frac{-B_f}{J_1 + m_2 l^2}\dot{\theta} + \frac{m_2 g l}{J_1 + m_2 l^2}\theta. \tag{3.36}$$

It can then be seen that

$$\omega_n^2 = \frac{m_2 g l}{J_1 + m_2 l^2} \tag{3.37}$$

and

$$2\zeta\omega_n = \frac{-B_f}{J_1 + m_2 l^2}. \tag{3.38}$$

The typical impulse response of a second-order system can be seen in Figure 3.21, which can be described by

$$\theta(t) = ke^{-\sigma t} sin(\omega_d t), \tag{3.39}$$

where σ is the real component and ω_d is the complex component of the second-order complex poles.

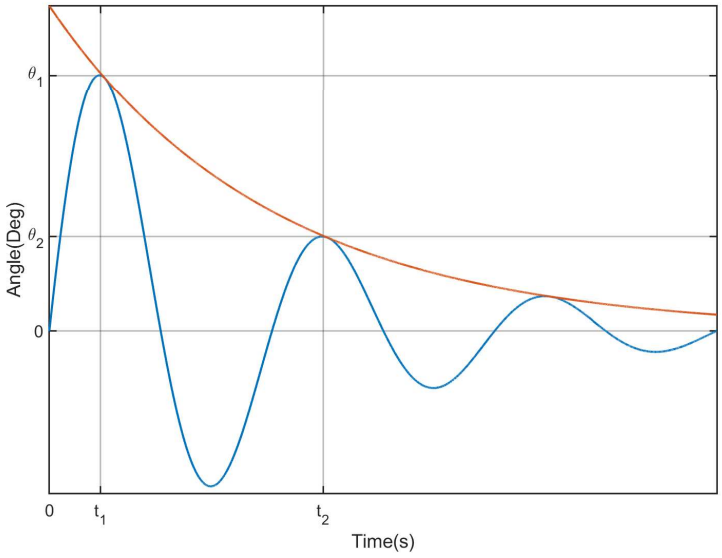


Figure 3.21: Second order system impulse response.

It can be seen from Figure 3.21 that at time t_1, $sin(\omega_d t_1) = 1$. This is the same for t_2 therefore,

$$\theta(t_1) = ke^{-\sigma t_1}; \quad \theta(t_2) = ke^{-\sigma t_2}. \tag{3.40}$$

From (3.40) the constant value k can then be eliminated through division as follows

$$\frac{\theta(t_1)}{\theta(t_2)} = \frac{ke^{-\sigma t_1}}{ke^{-\sigma t_2}} = \frac{e^{-\sigma t_1}}{e^{-\sigma t_2}} = e^{\sigma(t_2 - t_1)}, \tag{3.41}$$

which can then be rearranged to

$$\sigma = \frac{1}{t_2 - t_1} ln\left(\frac{\theta(t_1)}{\theta(t_2)}\right). \tag{3.42}$$

In order to determine ω_d it is known that a full oscillation is completed by the pendulum every 2π and thus,

$$\omega_d(t_2 - t_1) = 2\pi$$

$$\therefore \omega_d = \frac{2\pi}{(t_2 - t_1)}. \tag{3.43}$$

With values for σ and ω_d, it is then possible to calculate the natural frequency ω_n from

$$\omega_n = \sqrt{\omega_d^2 + \sigma^2} \tag{3.44}$$

and the damping ration ζ from

$$\zeta = \frac{\sigma}{\omega_n}. \tag{3.45}$$

Finally, by rearranging (3.37) and (3.38), J_1 can then be calculated from

$$J_1 = \frac{m_2 g l}{\omega_n^2} - m_2 l^2 \tag{3.46}$$

and B_f can be calculated with

$$B_f = 2\zeta\omega_n(J_1 + m_2 l^2). \tag{3.47}$$

Due to $sin\theta \approx \theta$ only holding for small angles, a pendulum with a relatively long length (l) was designed. This allows for greater potential energy in the system while maintaining small angles, as well as increasing the accuracy of the measurements.

Due to the high accuracy required in the angle measurements, a method was devised using a horizontal measuring instrument as seen in Figure 3.22.

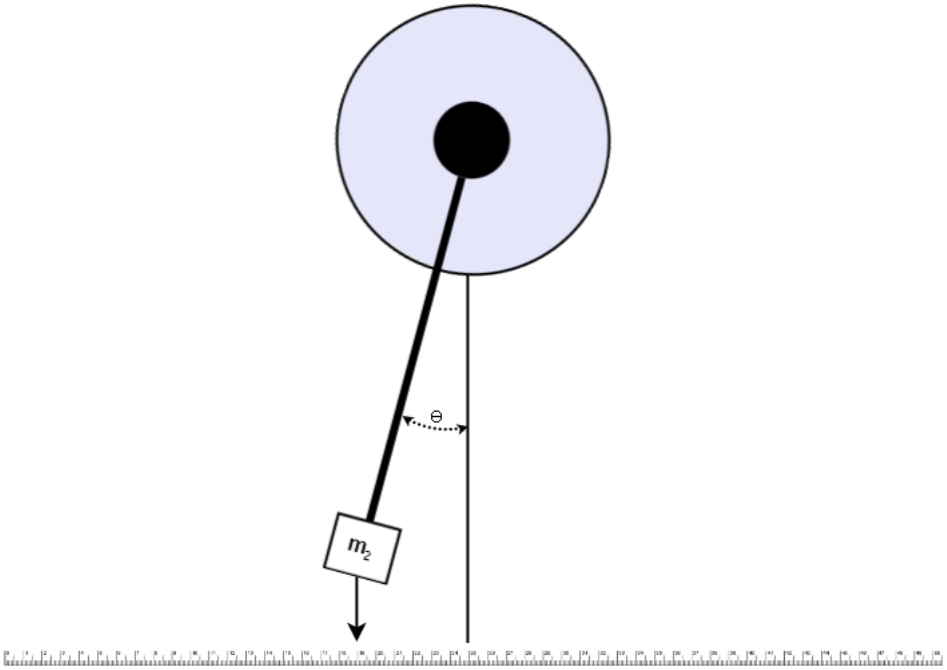


Figure 3.22: Pendulum angle measurement.

To ensure accurate time and angle readings were taken, the test procedure was filmed. This allows for an accurate frame by frame playback. Once the time values for t_1 and t_2 are identified the angles can then be calculated from

$$\theta = sin^{-1}\left(\frac{x}{l}\right) \tag{3.48}$$

where x is the measured distance from the centerline, and l is the length of the pendulum.

3.3.4 Field oriented control

Due to the advantages of FOC such as low torque ripple, high efficiency and high torque with low currents at start up, it was decided that this was the best control method to use for this design example [23]. These advantages and the operation of FOC are further discussed in detail in section 3.2.3.3. It is however important to note that any machine control method can be used in the process of the design methodology, FOC was only chosen for the design example due to its advantages suiting the specific application.

Within the Simscape Matlab package, a PMSM Field-Oriented Control module is available which can be seen in Figure 3.23.

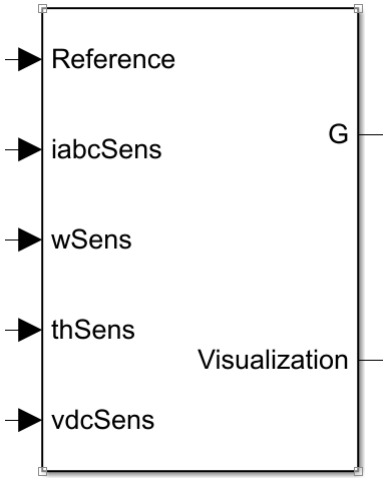


Figure 3.23: PMSM FOC module.

The FOC controller can be configured to follow a reference of torque in Nm or angular velocity in rad/s. This is supplied to the controller on the input labeled "Reference". Due to the aim of the simulation being current measurement and to determine the three-phase losses the reference is set to torque. Additionally, the controller also requires the measured rotor angle ($thSens$), phase currents ($iabcSens$) and supply voltage ($vdcSens$). From these input values, the controller calculates the required gate outputs which are supplied via output G.

The FOC control module makes use of two PI control systems, one for the control of the direct current and the other for the control of the quadrature current. These two PI control systems need to be configured to achieve an adequate torque output vs reference error.

3.3.5 Power measurement and machine load

To determine the input power, the instantaneous battery current and voltage are measured after which it is then multiplied. However, this results in the instantaneous input power

which has to be averaged over a time period. To achieve this a moving average filter is implemented with a window size of 1×10^6 samples. This method is chosen over a simple total average as it allows the startup power as well as any oscillations in power to be seen.

Due to the properties of a PMSM, the phase current is directly proportional to the torque output applied to the load. Therefore, the simulated load torque is to be adjusted in order to achieve an appropriate average input power. However, before the torque reference can be adjusted, the PI control system parameters of the PMSM FOC module have to be fine-tuned to achieve an acceptable torque ripple.

3.4 Choosing switching components

The first key specification to be set for choosing an appropriate MOSFET is the minimum drain-source voltage, keeping in mind non-ideal voltage transients.

The second MOSFET specification is the minimum safe operating drain current. Often the specified maximum current rating of a MOSFET is not reliably achievable. This is normally calculated using the maximum junction temperature and the on-state resistance by

$$T_{j-c} = 125 - T_A \tag{3.49}$$

and

$$I_{D(Max)} = \sqrt{\frac{T_{j-c}}{R_{\theta JC} \cdot R_{DS(on)}}}. \tag{3.50}$$

Therefore it is critical for the reliability of the inverter that the devices are kept within their safe operating area. In order to do this a figure such as Figure 3.24 must be found for the device. The typical V_{DS} across the MOSFET must be known, as well as the switching frequency to then determine which graph is applicable.

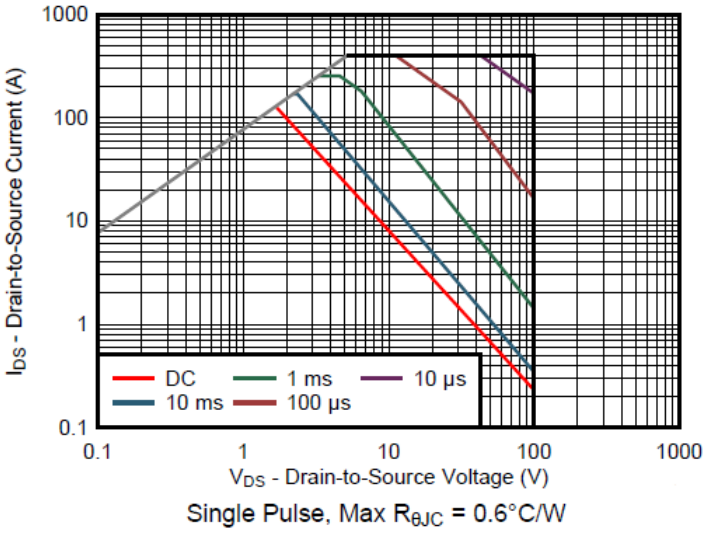


Figure 3.24: CSD19532KTT safe operating area.

Once the minimum required MOSFET specifications are set, the focus is then placed on MOSFET parameters which reduce losses. These parameters are the R_{DSon} value and the gate charges. A selection of MOSFETs from a number of different suppliers using different technologies should be chosen. This allows for a comparison between the technologies to find the best applicable for the application.

3.5 Example application

3.5.1 Determining currents though simulation

In order to ensure the current values simulated through the switches were accurate, an average power of 5 kW had to be confirmed. In this simulation, the input power can be approximated to the output power. This is because the switches operate as ideal with negligible losses.

The simulation was configured with the values seen in Table 3.1 which were calculated using the methods discussed in the sections above. For the current and voltage measurements to determine the phase resistance, two Fluke multimeters with an accuracy of less than $0.5\% \times (measured\ voltage) + 3$ mV and $1.5\% \times (measured\ current) + 3$ mA were used. A Tektronix TDS1002B oscilloscope was used to take the required measurements in order to calculate the direct and quadrature inductances.

To calculate the inertia and friction coefficient of the machine a pendulum with a length of 960 mm and weight of 512 g was used.

Table 3.1: Results from phase resistance tests.

Parameter	Value
$Pole\ Pairs$	3
L_d	26 μH
L_q	52 μH
J	0.097 $kg \cdot m^2$
B_f	$0.399 \frac{N \cdot m \cdot s^2}{rad}$
R_S	8 $m\Omega$

Figure 3.25 shows the simulated output torque for a ramped step response with a final value of 10 Nm. It can also be seen from Figure 3.26 that the PI control system is sufficiently tuned as there is an adequately low oscillating error with a average peak to peak value of approximately 0.68 Nm.

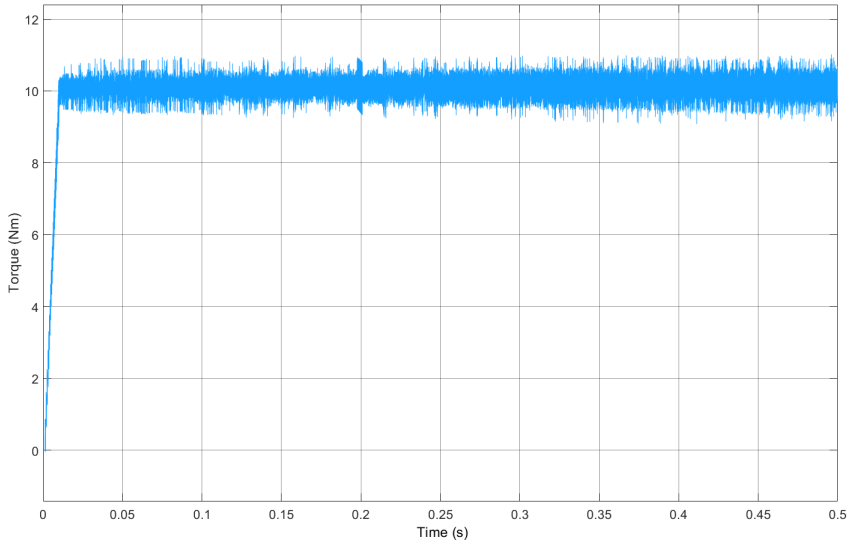


Figure 3.25: Output torque vs time for step response of 10 Nm.

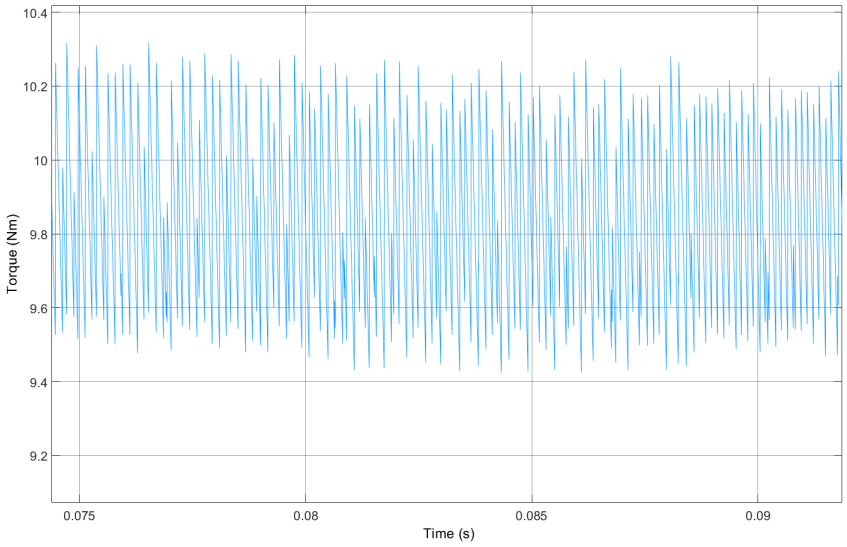


Figure 3.26: Torque ripple.

Additionally, from Figure 3.27 the 120° out of phase sinusoidal output currents can be seen which along with Figure 3.28 indicate the rotation of the PMSM.

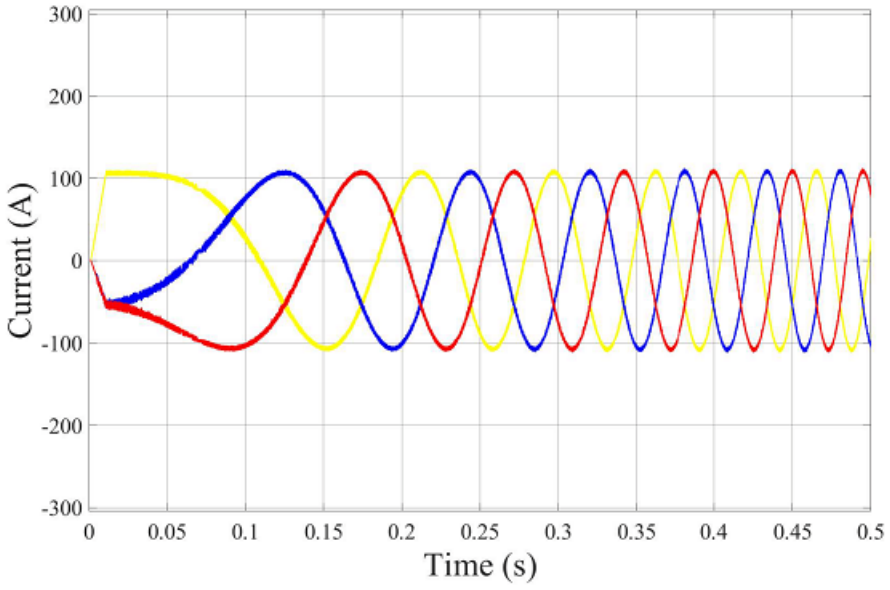


Figure 3.27: Phase currents with 10 Nm load.

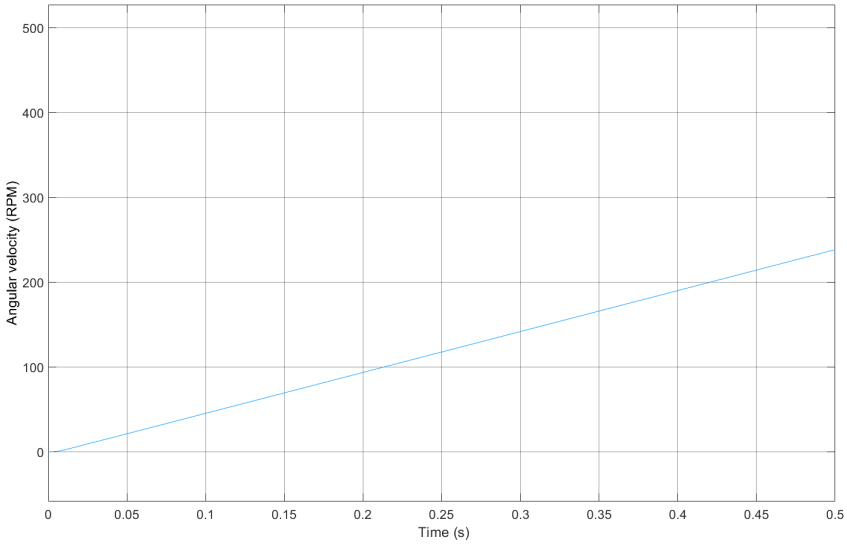


Figure 3.28: Angular velocity with 10 Nm load.

The output of the moving average filter applied to the instantaneous power measurement as discussed in section 3.3.5 can be seen in Figure 3.29 when a torque reference of 20 Nm was used.

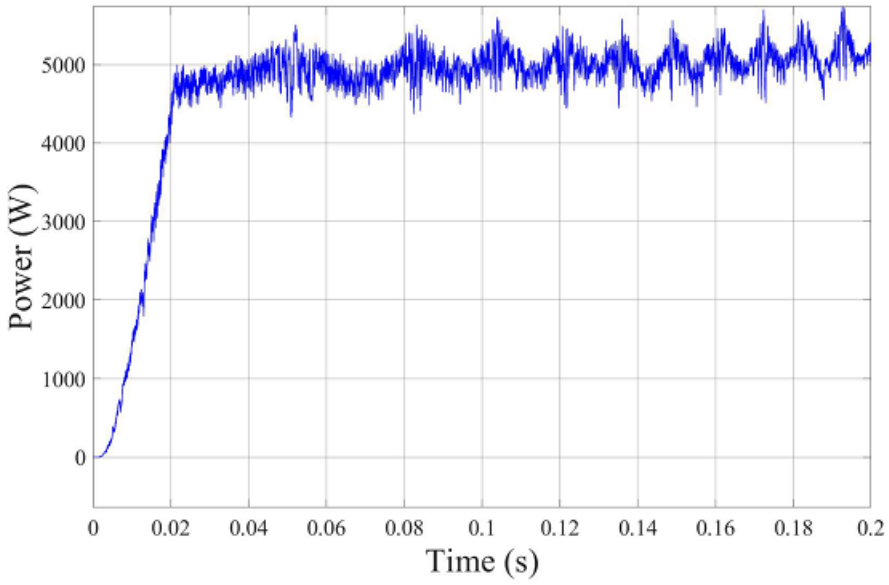


Figure 3.29: Input power after moving average filter.

After confirming that the simulated torque was constant and the input power is approximately equal to 5kW, the focus was placed on the switches within the inverter. The instantaneous drain current and drain-source voltage of a low side switch was investigated. From the investigation, Figure 3.30 shows a maximum instantaneous drain current of 219.6 A through the switch as well as a maximum drain-source voltage of 48 V.

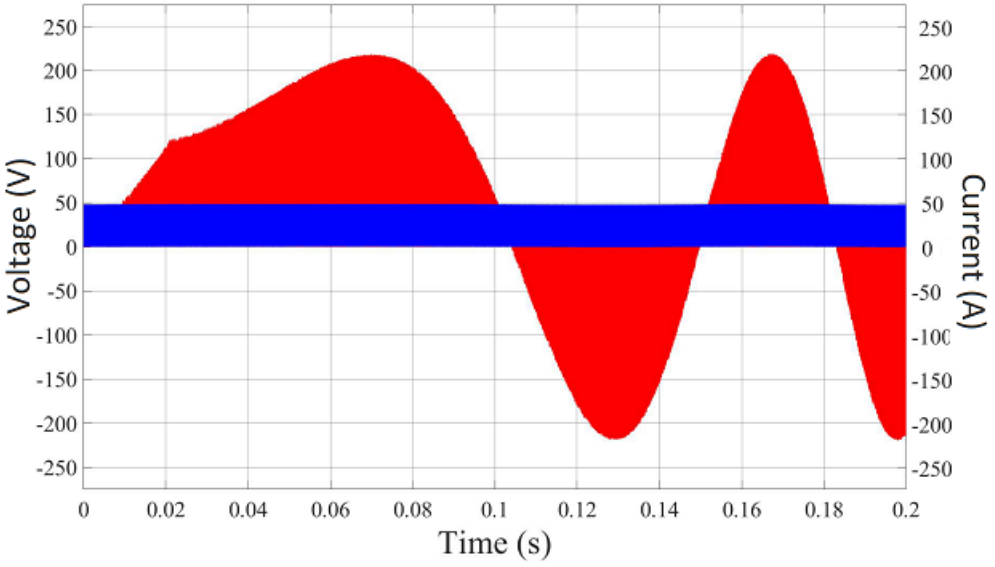


Figure 3.30: I_D and V_{DS} of low side switch.

Additionally, another moving average filter with a sample window size of 1×10^6 samples was used to filter I_D and V_{DS}. This is shown in Figure 3.31 and allows for an indication of the filtered current and voltage of the switch.

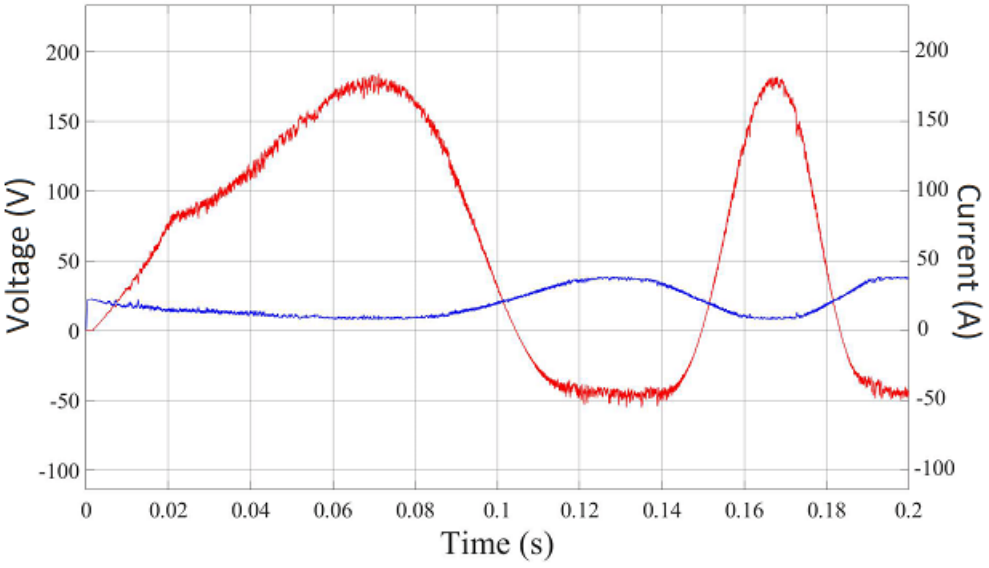


Figure 3.31: I_D and V_{DS} of low side switch after moving average filter.

3.5.2 Selecting switches using determined parameters

In the example application the frequency of which the inverter has been designed to operate at is between 10 kHz and 100 kHz. The higher switching period of 100 μs must be used to ensure that the device is in its safe operating area for all operating frequencies. From Figure 3.24 we can then see that for the CSD19532KTT device, the maximum safe operating

current for a V_{DS} of 56 V is approximately 40 A. Knowing the maximum peak drain current of 219.6 A and the safe operating current value, the number of devices required in parallel can be calculated. It was decided due to form factor constraints that no more than twelve devices could be placed in parallel.

A selection of seven suitable MOSFETs was made of which a parameter comparison can be seen below in Table 3.2. This MOSFET selection is comprised of choices from multiple different semiconductor manufacturers thus, allowing the comparison between different MOSFET technologies such as:

- Vishay's ThunderFET®
- Nexperia's TrenchMOS technology™
- Texas Instrument's NexFET™
- STMicroelectronic's STripFET™
- Fairchild's QFET®
- Infineon's OptiMOS™

Table 3.2: Suitable MOSFET parameters.

Device	On State resistance($m\Omega$)	Gate charge(nC)	Operating current(A)	Thermal resistance(°C/W)
IPB083N10N3	8.2	55	20	1.2
BUK7626-100B	26	38	45	0.95
FQB44N10TM	30	50	80	1.03
STB35NF10	35	55	35	1.3
CSD19535KTT	2.8	75	60	0.5
CSD19506KTT	2	120	100	0.4
CSD19532KTT	4.6	44	40	0.6

3.6 Simulation to determine losses

3.6.1 Section overview

The aim of this set of simulations is to investigate losses in the MOSFET switches. This is done to perform a comparison between different MOSFET options. By simulating the different MOSFET options a good compromise can be made between cost, efficiency, reliability and form factor.

All of the simulations to determine losses are run for switching frequencies of 10 kHz, 50 kHz and 100 kHz to help aid in the choice of final switching frequency. Due to a short delay at startup as well as the torque of the motor following a ramp reference, the beginning of the simulation is omitted. By doing this, the data used was a more accurate representation of a constant running state.

3.6.2 Implementing MOSFET choices

The simulation model of the three-phase inverter can be seen in Figure 3.32, where each of the six switches as well as their gate drivers are represented in subsystems.

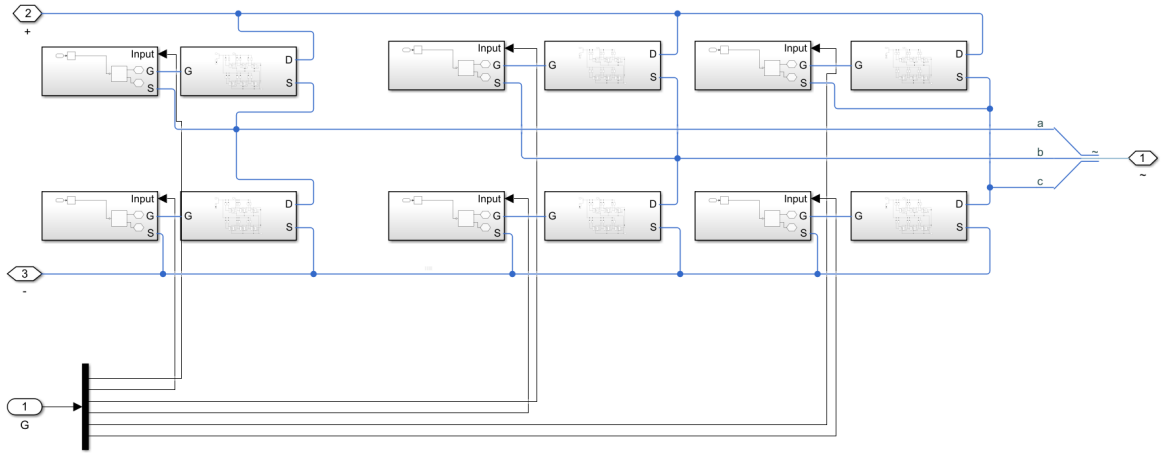


Figure 3.32: Three-phase inverter model.

Each of the six single switch subsystems is then modeled as seen in Figure 3.33 in which MOSFETs can be added in parallel for the design application.

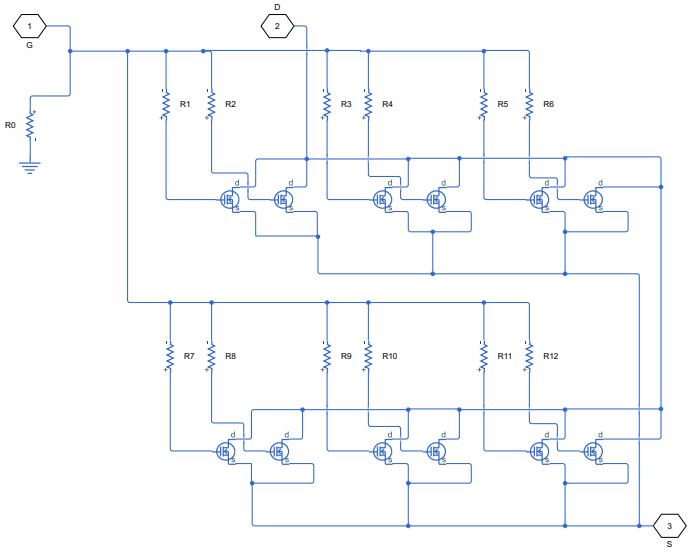


Figure 3.33: Single switch subsystem.

In order to accurately simulate the turn-on and turn off times which are fundamental for the switching losses gate resistors are added as mentioned in section 3.2.6. Additionally, the MOSFET properties are set along with gate driver parameters such as output resistance and output voltage.

3.6.3 Simulating losses

To test the accuracy of the switching losses a simulation as seen in Figure 3.34 is used. In this simulation a square wave signal is the input into the gate driver subsystem. The aim of this simulation is to view the voltage and current profiles during the switching times.

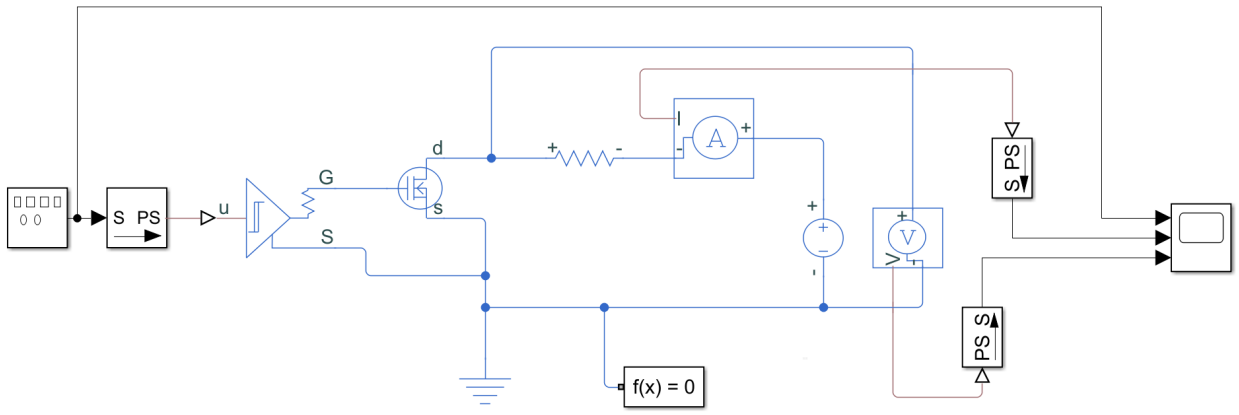


Figure 3.34: Switching losses simulation.

The results of this simulation are presented in figures 3.35 and 3.36 where it can be seen that the voltage and current in each figure changes simultaneously unlike in Figure 3.12. From this comparison it is clear that the simulated on and off switching voltages and currents are not correct. Therefore, the MOSFET gate capacitances are kept as 0 pF making the switching losses 0 W. The switching losses are then calculated separately following the strategy of injecting the switching losses into the simulation.

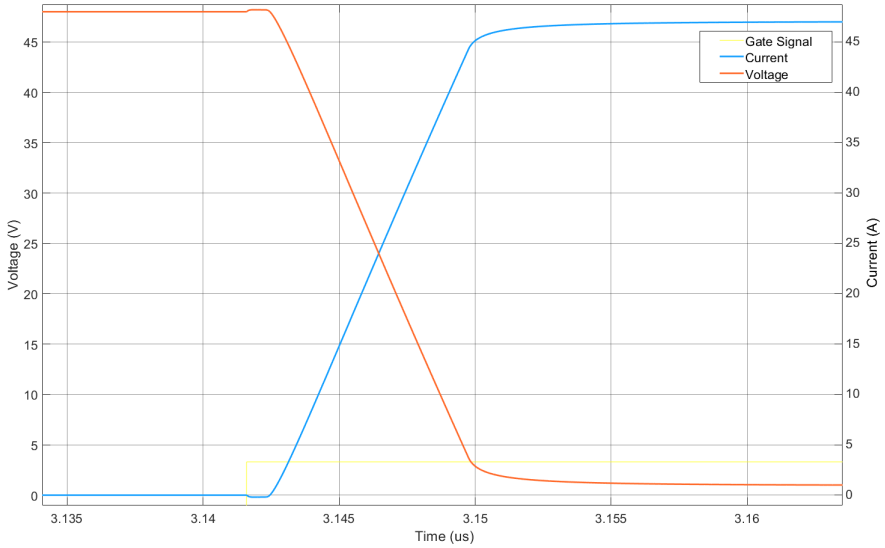


Figure 3.35: Turn-on period.

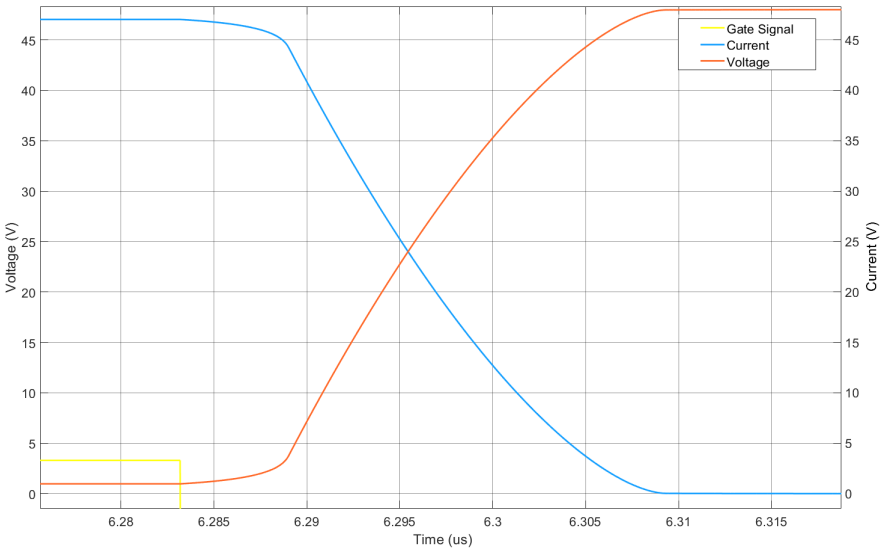


Figure 3.36: Turn off period.

Due to the switching losses now being negated it is required to remove the simulated conduction losses for the time period over which switching should have taken place. This is done by adding a turn-on delay to the MOSFET drivers. The length of this delay is set to the summation of both the turn-on and turn off times.

To attain the switching losses from the simulated currents, the switching times need to be calculated from the equations derived in section 3.2.5.2. In order to do this, equivalent values for the gate resistance, drain to gate capacitance and gate to source capacitance have to be determined. Due to the MOSFETs being in parallel the equivalent gate resistance of the switch subsystem can be calculated as

$$R_{G(eq)} = \frac{R_{gate}}{N} + R_{Driver}, \tag{3.51}$$

where $R_{G(eq)}$ is the equivalent gate resistance, R_{gate} is the individual gate resistance, R_{driver} is the resistance of the gate driver and N is the number of MOSFETs placed in parallel. The equivalent drain to gate capacitance ($C_{dg(eq)}$) and gate to source capacitance ($C_{gs(eq)}$) can be also calculated as

$$C_{dg(eq)} = C_{dg} \times N; \quad C_{ds(eq)} = C_{ds} \times N. \tag{3.52}$$

Once the switching times have been determined the MOSFET current and voltage is needed before and after each switching occurrence. For this reason the current and voltage for a single switch subsystem is measured, each of which is then written to a CSV file. The CSV files are configured to be of two dimensions, these being time and the measured value. Figure 3.37 below shows the Matlab Simulink model which is used to do this.

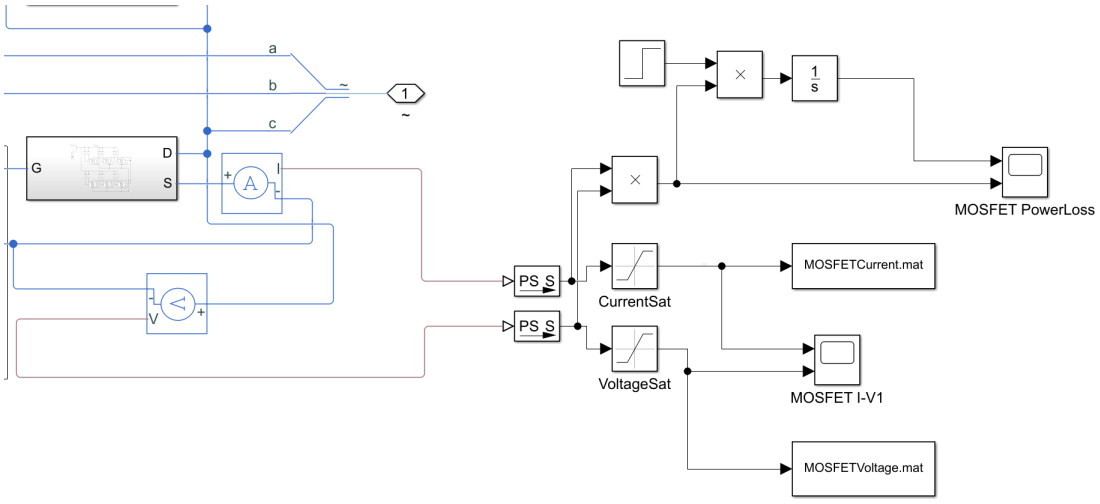


Figure 3.37: Matlab Simulink model of inverter measurement setup.

A Matlab script is used to cycle through every element of the array and identify switching sates. A switching state is identified by the voltage crossing a threshold of 24 V. This is achieved by comparing every sample with the sample before it. If one sample is greater than or equal to 24 V and the other lower, a switching state has occurred. By noting which sample was lower than 24 V, it can also be identified whether it was an on or off switching event.

Once a switching event has been identified, a sample of the voltage and current from either side of the switching event is taken. These values are then used along with the switching times to calculate the losses for the event. The losses for the single event are then added to the total switching losses after which the average switching losses are then calculated.

Due to the fact that voltage and current being analysed by the Matlab script is only measured from one switch subsystem, the average switching losses have to be multiplied by six. This then results in the total average switching losses for the entire three-phase inverter. The total average switching losses for each MOSFET configuration can be seen in Table 3.3. In theory the switching losses should be directly proportional to the switching frequency, however due to additional factors such as the current ripple within the machine they are not exactly linear. In some cases such as the IPB083N10N3 the switching losses at 100 kHz are substantially non linear with a 22.4 W difference from theoretical which is more than 50 % of the conduction losses. This non linearity should be studied in more detail however, it is not necessary for the purpose of the design methodology.

Table 3.3: Average switching losses.

Device	Average switching losses (W)		
	10 kHz	50 kHz	100 kHz
IPB083N10N3	68.79	338.38	665.45
BUK7626-100B	43.78	214.53	413.07
FQB44N10TM	16.39	80.74	151.51
STB35NF10	45.28	221.90	427.22
CSD19535KTT	41.77	205.46	404.21
CSD19506KTT	71.81	353.42	695.81
CSD19532KTT	30.97	152.32	299.56

To determine the total losses, the conduction losses are also required. This is done by using the same current and voltage sensors used to take the measurements for the switching losses. The output from the two sensors is then multiplied together, which results in the instantaneous conduction losses. To determine the total energy lost due to conduction, the instantaneous losses are fed into an integrator. This is then divided by the time over which the integrator ran, thus resulting in the average conduction losses for one switch subsystem. After multiplying this value by six the total average conduction losses for the inverter are known. These values can be seen in Table 3.4 below.

Table 3.4: Average conduction losses.

Device	Average conduction losses (W)		
	10 kHz	50 kHz	100 kHz
IPB083N10N3	54.94	52.31	44.21
BUK7626-100B	354.72	342.96	289.44
FQB44N10TM	626.40	610.60	530.40
STB35NF10	357.36	346.08	291.80
CSD19535KTT	55.34	54.48	44.90
CSD19506KTT	39.52	38.67	31.80
CSD19532KTT	60.60	59.18	48.79

To get the total losses within the three-phase inverter the switching and conduction losses were simply added, the results of which can be seen in Table 3.5.

Table 3.5: Total losses.

Device	Total losses (W)			Parallel
	10 kHz	50 kHz	100 kHz	MOSFETs
IPB083N10N3	123.73	390.69	709.66	12
BUK7626-100B	398.50	557.49	702.51	6
FQB44N10TM	642.79	691.34	681.91	4
STB35NF10	402.64	567.98	719.02	8
CSD19535KTT	97.11	259.94	449.11	4
CSD19506KTT	111.33	392.09	727.61	4
CSD19532KTT	91.57	211.50	348.35	6

From the results attained it can be seen that a high component count, such as for the IPB083N10N3 does not result in a significant reduction in losses and thus is not worth the additional cost. It is clearly seen that some devices are designed optimally for high frequency applications such as the FQB44N10TM however, they have high conduction losses which ofset this advantage. Thus, a device with a good compromise between switching losses and conduction losses must be chosen. Such devices are the CSD19535KTT and CSD19532KTT where it can be seen that the CSD19532KTT is overall the most efficient MOSFET choice resulting in a 95.78% efficiency. However, the CSD19532KTT requires six parallel MOSFETs, whereas the CSD19535KTT only requires four. Thus, a design decision needs to be made regarding the compromise between slight improvement in efficiency vs the additional component count and thus cost.

It can also be seen that the switching losses comprise the majority of the total losses for frequencies of 50 kHz and above. Thus, a compromise has to be made between smoother

motor torque reducing audible noise and total losses when choosing a switching frequency. It is recommended to not have the switching frequencies below 20 kHz as the audible range of humans is approximately between 20 Hz and 20 kHz. Additionally the torque ripple below 20 kHz will result in a higher noise amplitude [24, 25].

3.7 Chapter summary

Chapter 3 begins with a literature review covering a number of topics used in following sections. After the literature review, block 3 in Figure 2.1 is completed by determining the requirements of the switching components through the simulation of a VSD and a PMSM. A selection of switching components are then chosen and applied to the example application. This allowed for a set of simulations to be completed to determine the losses for each switching component. With the completion of these simulations, block 4 of Figure 2.1 is now partially completed and can be completed in the following chapter.

Chapter 4

Thermal simulations

4.1 Introduction

It is common practice in engineering when a parameter such as maximum temperature or stress is unknown, to implement a safety factor ensuring critical failure will never be reached. In many cases the thermal aspect of the design is an example of this with it being an afterthought and not a priority. This methodology typically places the focus purely on not exceeding a components maximum temperature and not on optimising to achieve the lowest possible temperature. As a result, the exact temperature of the design is often not known which can lead to a reduction in reliability and a non-ideal design or cooling solution, due to safety factors which have to be implemented. By concurrently designing the thermal and electric aspect of the design, the risk and design time is greatly reduced [26].

The aim of this chapter is to place the thermal element at the forefront of the VSD design, enabling the thermal optimisation and comparison between different concept PCB's. By using the method presented in this chapter the engineer is able to choose the layout that best meets, or exceeds the design requirements [26].

The chapter begins with a short literature review on a number of topics required for the understanding and completion of the thermal simulations. Following this the computational fluid dynamics simulation package is briefly discussed. To ensure that the thermal simulation of the three-phase inverter is accurate, a single MOSFET is simulated under a known set of conditions. This allows for the confirmation that the simulation results will be sufficiently accurate. After confirming the simulation of a single MOSFET, four PCB designs are optimised to reduce hot spots. Finally using the information attained in the previous chapter, thermal simulations are run to determine the best choice of switching component.

External design factors such as the heatsink are not focused on in this thesis. This is due to the variation in cooling methods required by the end users application. Examples of these cooling solutions are an air-cooled heatsink or liquid cooling with the use of a radiator. However, the thermal resistance of the VSD is determined through simulation, allowing the end user to choose a sufficient cooling solution which best suits their application.

4.2 Literature related to thermal simulations

4.2.1 Literature overview

In this literature review the use and methods of thermal simulations in electronic designs are briefly discussed. After this two key factors in thermal design are focused on, these being

the PCB and thermal interface materials.

4.2.2 Thermal effects on reliability

The steady state temperature as well as the temperature cycling of semiconductor components makes up 55% of the total stresses for power electronic equipment, and 21% of the device failure distribution [27, 28]. Due to this it is known that high temperatures are the primary cause of failure and reduction in semiconductor life span [29–31]. Additionally, temperature cycling can cause failures due to solder fatigue. This is due to the difference in thermal expansion rates between the copper PCB traces and the silicon die, resulting in shear stresses being placed on the solder joints [28, 32]. This solder joint failure rate is not only correlated to the temperature variation but also the temperature ramp rate [33]. All of this points to the importance of reducing the hot spots within the design of power electronics, ultimately improving reliability.

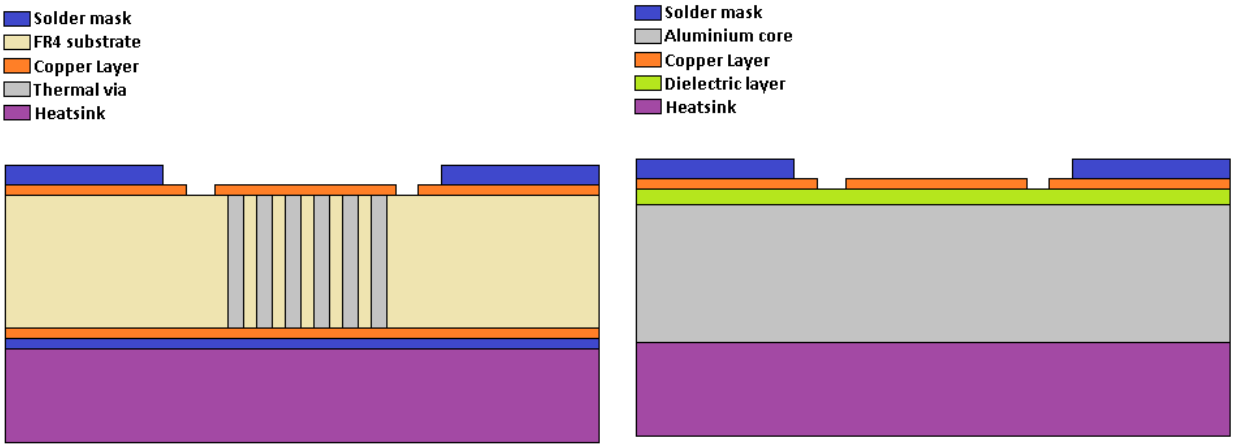
4.2.3 Thermal simulation using modular design

The most accurate method to determine the thermal aspects of a power electronic design is to incorporate the finite element method (FEM) with the electronic simulation. By using this method, component properties such as the variance in gate turn on voltage due to temperature can be included [34]. However, this method of integrating the thermal FEM simulation with the electronic simulation results in a non practical simulation time [35]. This is due to a relatively fast FEM simulation taking a minimum of a number of seconds per electrical simulation step [36]. Thus, with a electrical simulation having thousands, possibly millions of simulation iterations a second, the simulation would take an unfeasible amount of time.

To reduce the simulation time, a preferred strategy is used in which the electrical and thermal simulations are isolated. This allows for a great reduction in the simulation time at the compromise of simulation accuracy.

4.2.4 Printed circuit board

For the power stage of the inverter, there are two main options with regards to the PCB substrate, these being FR4 or metal-core. Typically when an FR4 substrate is used, thermal vias are placed below and or around the component, to aid in the transfer of heat between layers. This can be seen in Figure 4.1a, where there are thermal vias between the two layers. This is needed as the FR4 substrate is made from a fiberglass composite which has an inherently bad thermal conductance. With a metal core PCB, the substrate itself has a good thermal conductance, thus removing the need for thermal vias and improving the overall heat dissipation. The consequence of this however, is the inability to have any vias through the PCB. This limits the design to having only surface mount components on one side of the PCB [37]. In applications where the entire bottom layer of the PCB is in contact with the heat sink, this is not an issue. However, in some applications, the heat sink is only in contact with the PCB at the localised area where heat must be dissipated, resulting in a metal-core PCB being non-ideal



(a) FR4 substrate PCB with thermal vias. (b) Aluminium core PCB.

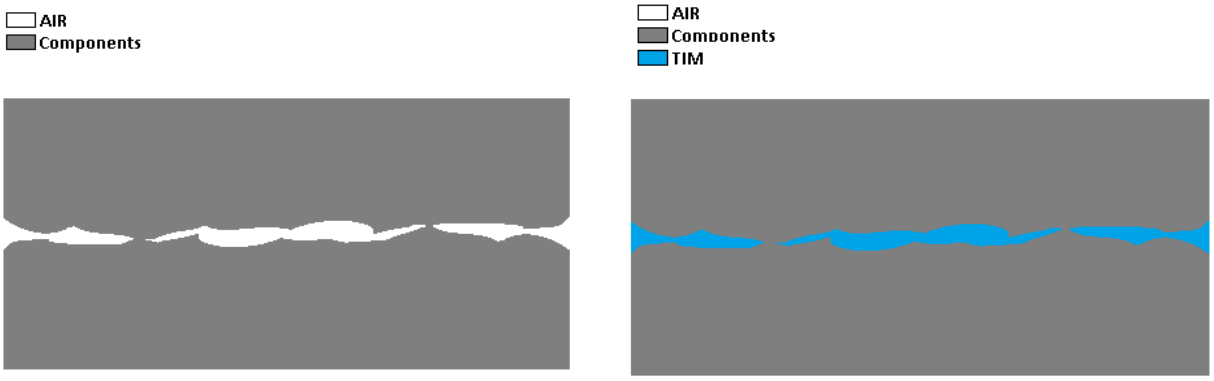
Figure 4.1: Cross-sectional comparison between PCB substrates.

As can be seen in Figure 4.1b there is a dielectric between the copper layer and the aluminium core, forming the required isolation [38]. As a result of this dielectric layer, the thermal conductivity between the copper layer and the core is reduced. Typically, the dielectric has a 0.1 mm thickness and a thermal conductivity of between 1 W/m·K and 3 W/m·K [39].

4.2.5 Thermal interface material

A thermal interface material (TIM) is any material placed between two objects to improve the thermal conductance of the mating surfaces. Typically this is done between a device that produces thermal energy such as a CPU and another that dissipates the thermal energy such as a heat sink [39].

The reason why TIMs are used is due to the tiny imperfections on a surface which can be seen at a high magnification, even when a surface appears smooth. These grooves cause a number of small air gaps between the two components, thus reducing the thermal conductivity of the mating surfaces. The TIM is used to fill the small gaps with a compound that has a much better thermal conductivity than air as seen in Figure 4.2.

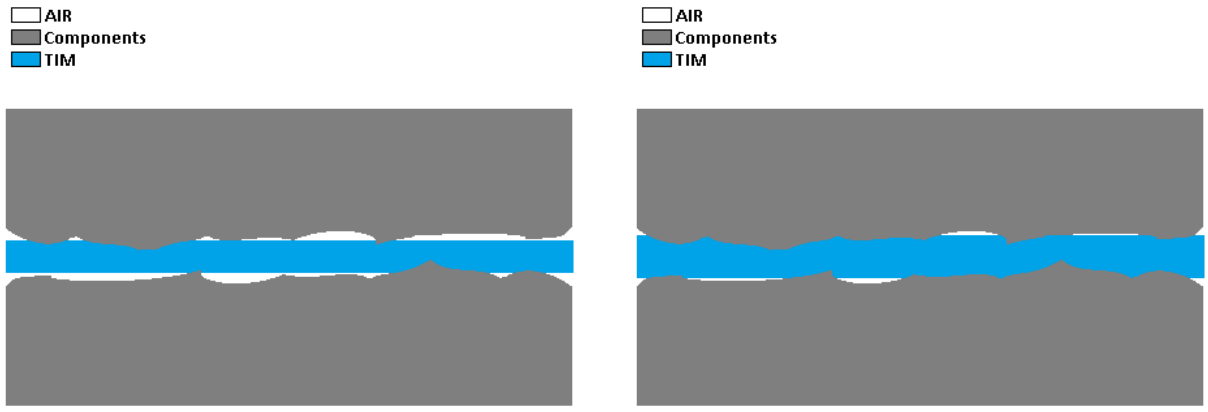


(a) Gaps filled with air. (b) Gaps filled with TIM.

Figure 4.2: Highly magnified cross-section with and without TIM to fill surface grooves.

There are a number of different TIM types, the most common of which are thermal pads, phase change materials and thermal grease. Each of these comes at a compromise of cost, effectiveness and ease of use within the manufacturing process.

Thermal pads or films are typically made from polymerized silicone rubbers and are ideally suited for user-friendly applications that require a neater final product. Additionally, thermal pads can be used in applications where isolation is required between two surfaces. The downside to thermal pads is that they are most effective with a force applied to them. This is due to the fact that the force reduces air gaps as seen in Figure 4.3. This force cannot always be applied easily, or with some components it cannot be applied at all due to strength issues. It can also be seen in Figure 4.3b where a high force is applied that there may still be small air gaps remaining [40].



(a) Light force applied. (b) High Force applied.

Figure 4.3: Thermal pad air gap.

From this information, it can be seen that thermal pads are ideally suited for applications where isolation is required. This can however, come at the compromise of a reduction in thermal conductivity if high forces cannot be applied.

Phase change materials are very similar in concept to thermal pads, and maintain the ease of handling but aim to remove the required high forces. This is achieved by the phase change material representing a film or pad at room temperature. However, once the device reaches operating temperature the film changes to a flowable phase. This allows the large air gaps caused by low forces as seen in Figure 4.3a to be filled easily.

Thermal Greases are made from a silicon or hydrocarbon oil base which has conductive fillers added to them. They are typically viscous fluids which allows them to fill voids extremely well with very little force required. This does however mean, that the manufacturing process is very untidy and potentially difficult. Typically in applications where the thermal mating surfaces are large or complex, thermal grease is the ideal TIM to use. This is due to the lower cost and easy profile adaptation.

4.3 AutoDesk CFD

Autodesk CFD is a computational fluid dynamics package, which allows the simulation of both fluid dynamics and thermal dynamics. For the application in which this chapter will utilise Autodesk CFD, only the thermal dynamics functionality will be focused on. This

is due to the fact that airflow over the VSD cannot be guaranteed, and thus forced air convection cooling cannot be counted upon.

The general procedure for running a thermal simulation starts off with the development of a CAD model. This can be done in many different software packages such as SolidWorks and Autodesk 360. However, it was decided for this application that Autodesk Inventor was the appropriate CAD modeling tool to use due to its capabilities of importing files directly from Altium. Once the CAD design was completed and launched into Autodesk CFD, the geometry tools were used to remove negligible edges and small objects. This was done to reduce the simulation complexity and thus simulation time. Additionally, the geometry tools were used to place a large air volume around the three-phase inverter, replicating the open atmosphere.

The next step in the configuration process is to set the materials of each element within the design. There are two main types of materials that can be set these being fluids and solids, of which only the air volume in our designs will be set as a fluid. There is a third material type, which is a surface material property known as contact resistance. This will be used to create the junction to case thermal resistance within the MOSFET. The material properties play a large role in the thermal simulations due to their thermal conductance values. After the materials are set, the boundary conditions for the simulation, such as total heat generation and ambient air temperature must be configured. If there are any initial conditions that need to be set, they will be set at this stage. However, for the simulations required in this chapter no initial conditions are needed. The configuration of the simulation is then complete and the next step is to create the mesh of the model.

Prior to analysis taking place in Autodesk CFD, the geometry must be broken up into small pieces known as elements. In 3D models, the elements are generally in the form of a tetrahedral, an example of which can be seen in Figure 4.4. The tetrahedral has four corners known as nodes, these are the points at which the calculations take place.

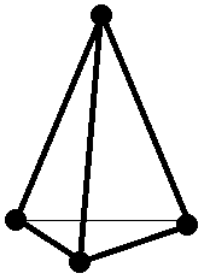


Figure 4.4: Tetrahedral with four nodes.

Fortunately, within Autodesk CFD there is an automatic mesh sizing tool which analyses the model and applies a mesh with varying sized nodes. In some applications, primarily where there are very small elements, the mesh sizing must be manually adjusted. This was not the case in the simulation of the three-phase inverter and thus, the automatic mesh sizing was adequate.

Once the setup of the simulation is completed the simulation solver must be configured. Within the simulation solver, there are multiple physics parameters that can be set under the sections of *Flow* and *Heat Transfer*. Due to the primary focus for the simulations in this chapter being on heat transfer, both the *Auto Forced Convection* and *Radiation* options are enabled.

The simulation within Autodesk CFD is run in an iterative manner, in which the values for each node are calculated repetitively. This is done for a set number of iterations or until the values calculated converge to a stable equilibrium. Therefore, to achieve the most accurate results a very high number of iterations should be configured allowing the simulation to fully run until it converges. It is however, recommend to set the iterations to a low value such as 100 for the first simulation run. This is done to limit the first simulation run time allowing any errors in configuration to be fixed early on.

A very useful feature offered in the Autodesk CFD solver is the ability to run the simulation on a separate local computer or on the cloud. Additionally, multiple simulations can be scheduled to run after each other or at specific times. These options allow the lengthy simulations to effectively run in the background whilst other simulations are configured.

4.4 Thermal simulation of one MOSFET

The thermal model of a single MOSFET has to be confirmed in order to ensure the accurate simulation of the three-phase inverter. The only detailed thermal information one can get from a MOSFETs datasheet is its thermal resistance values. Due to the MOSFET being mounted to a heatsink, the junction to case thermal resistance value ($R_{\theta j-c}$) is used.

A simple test simulation which can be seen in Figure 4.5 below is configured. This simulation uses a single MOSFET mounted to a 50 mm x 50 mm x 3 mm aluminium heatsink. The MOSFET and heatsink are placed in a large air volume with boundaries set to a room temperature of 25° C.

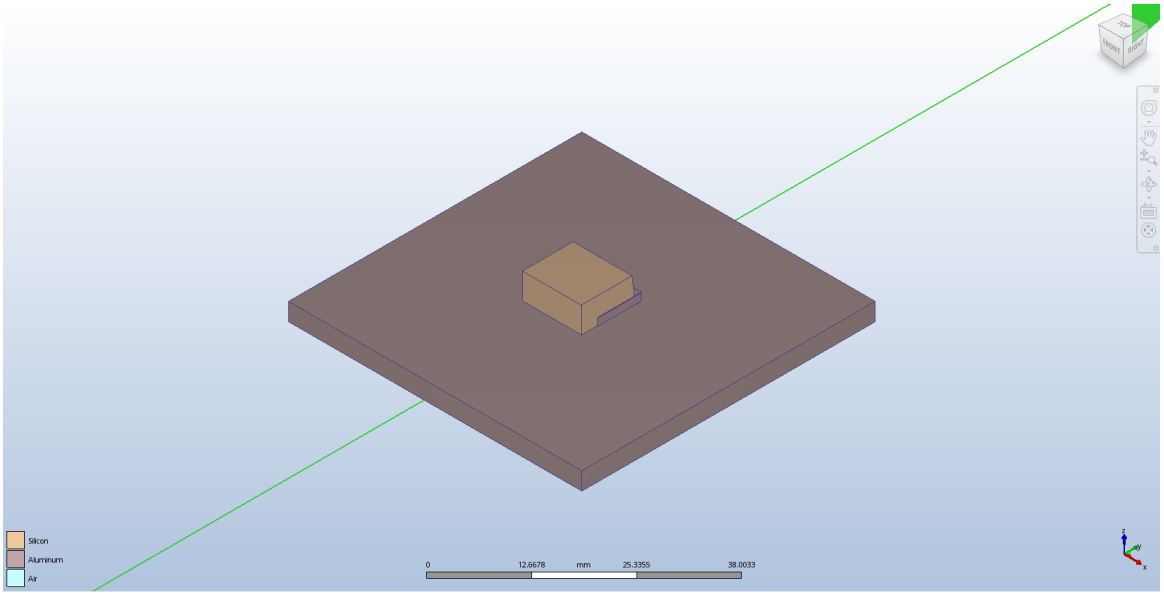


Figure 4.5: MOSFET thermal model test setup.

To test the MOSFETs thermal model, using the value of $R_{\theta j-c}$, the principle of an infinitely large heat sink is used. This is done by setting the top surface of the heatsink to a fixed room temperature of 25 °C.

To create a thermal resistance in Autodesk CFD, the material of type contact resistance is applied to the surface in which the thermal resistance is desired. This can be seen in Figure 4.6, where the contact resistance surface is light blue. The unit for the value of the contact resistance is °K·mm^2/W. Therefore to relate this to the thermal resistance value from the

datasheet given in °K/W, the area of this surface must be calculated. A value of 0.5 °K/W is chosen for this test, thus with a surface area of 75.249 mm^2 a value of 37.6245 °K·mm^2/W is calculated.

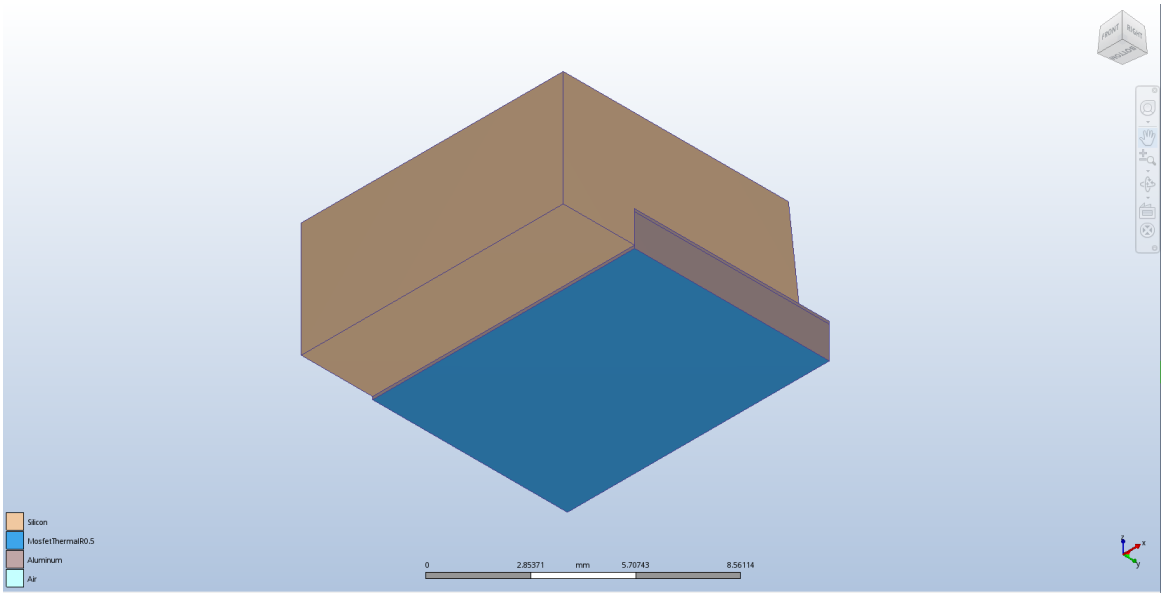


Figure 4.6: MOSFET contact resistance.

A boundary condition of type "Total Heat Generation" is added to the volume which can be seen in Figure 4.7 is as red. This boundary condition allows the total amount of heat generation to be set in watts.

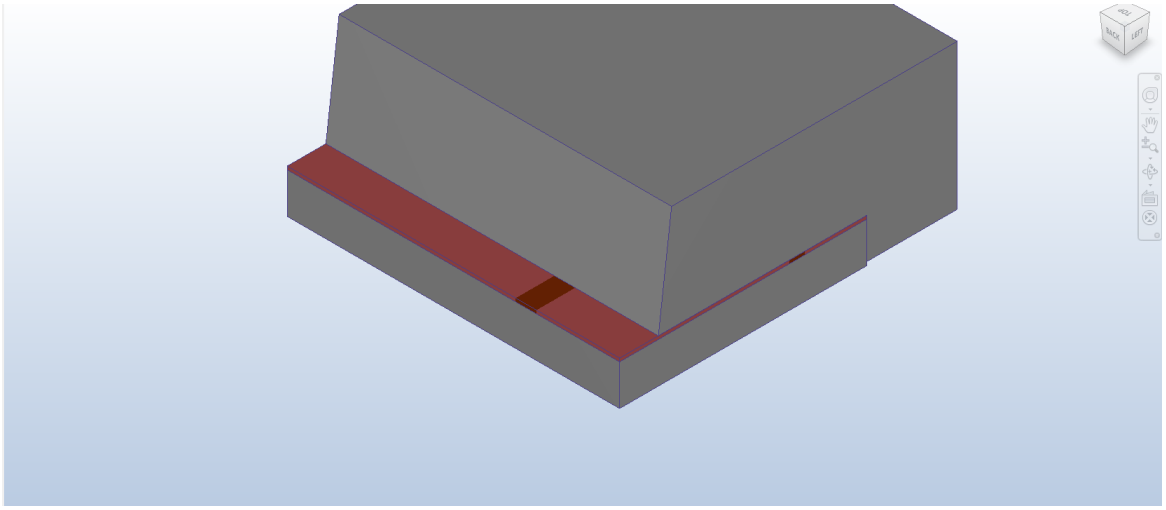


Figure 4.7: MOSFET heat generation boundary condition.

Choosing a $R_{\theta j-c}$ value of 0.5 °K/W, an ambient air temperature of 25 °C and a power of 15 W, a theoretical maximum temperature can be calculated as

$$T_{max} = 25 + 0.5 \times 15 = 32.5\ ^\circ C. \tag{4.1}$$

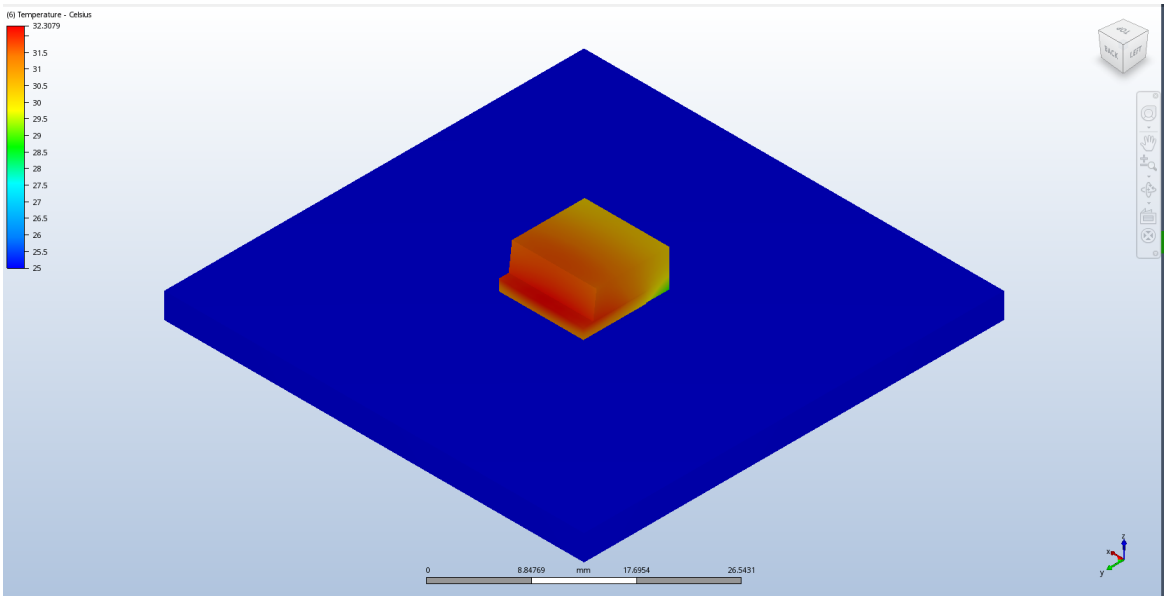


Figure 4.8: MOSFET model simulation result with a maximum temperature of 32.308 °C.

From Figure 4.8 it can be seen that a maximum temperature of 32.308 °C is simulated. To investigate the difference of 0.192 °C between the theoretical value and simulated value, the ambient air temperature and power losses are varied.

To do this, the simulation is first run multiple times with a variation of ambient air temperatures, the results of which can be seen in Table 4.1. From these results and the known theoretical temperatures, it can be seen that the difference between the calculated and simulated temperature remains fairly constant. Thus, ambient air temperature can be ruled out as the cause for the 0.192 °C difference.

Table 4.1: Simulated and calculated temperatures for a variation of ambient temperatures.

Ambient temperature(°C)	Max temperature(°C)	Expected result(°C)	Difference(°C)
20	27.308	27.5	0.192
25	32.308	32.5	0.192
30	37.333	37.5	0.167
35	42.334	42.5	0.166
40	47.334	47.5	0.166
45	52.333	52.5	0.167
50	57.308	57.5	0.192

The simulation is rerun with the ambient air temperature kept constant at 25 °C, and the heat dissipation power level varied. The results of these simulations can be seen in Table 4.2 where it is clear that the power level and error are proportional. Regardless of this, the error remains below 3% at 25 W thus, the simulation is considered sufficiently accurate for the design methodology.

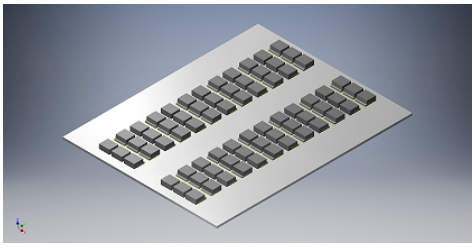
Table 4.2: Simulated and calculated temperatures for a variation of total heat generated.

Power (W)	Max temperature(°C)	Expected result(°C)	Difference(°C)
1	25.487	25.5	0.013
5	27.436	27.5	0.064
10	29.871	30	0.129
15	32.3079	32.5	0.1921
20	34.744	35	0.256
25	37.1798	37.5	0.3202

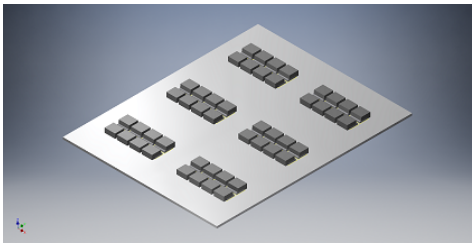
4.5 PCB development with thermal simulation

After confirming the acceptable accuracy of the thermal model created for a D2Pack MOSFET. The model can be used to simulate the thermal effects within the three-phase inverter. The primary focus of the thermal simulations in this section is to design a thermally optimal PCB for each choice of switching component. This will conclude block 4 in Figure 2.1 which was started in the previous chapter.

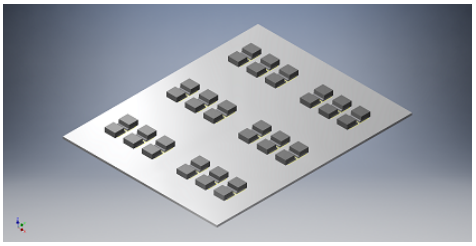
Due to the difference in MOSFET safe operating currents between switching component choices, a different number of MOSFETs are required in parallel. Therefore, four different CAD models were designed, these can be seen in Figure 4.9. Each of the four designs were placed through the process of simulation, after which the results were analysed for hot spots. If possible, improvements were identified and then implemented before re-simulating the design to confirm their effects.



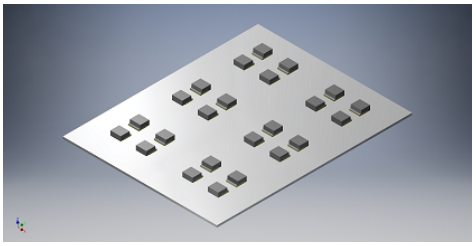
(a) 72 MOSFET option.



(b) 48 MOSFET option.



(c) 36 MOSFET option.



(d) 24 MOSFET option.

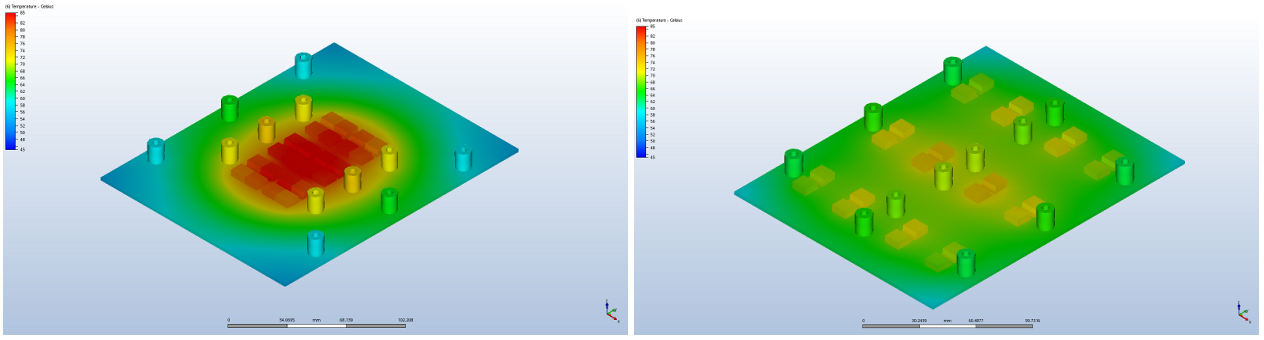
Figure 4.9: MOSFET PCB CAD models.

To ensure the validity of the thermal simulations, the following set of control factors are established. The total heat generation between all MOSFETs is 96 W due to this being in the range of practical losses. The ambient air volume must be set to 1 m^3 as this is large enough to allow the air temperature around the PCB to converge thus, simulating open atmosphere. The boundaries of this ambient air volume must be set to a constant temperature of 25 °C. There must be 12 power element standoffs with material of type

Copper placed on the PCB. And finally, the junction to case thermal resistance of each MOSFET must be 0.5 °C/W.

The values chosen for all of these control factors are of no direct importance to the optimisation of the PCB, however it is critical that they are kept constant.

A number of key design recommendations were soon identified after completing a series of simulations. The first of which is shown in Figure 4.10, where it can be seen that good space distribution of the MOSFETs across the PCB reduced the total temperature by 13.74 °C.

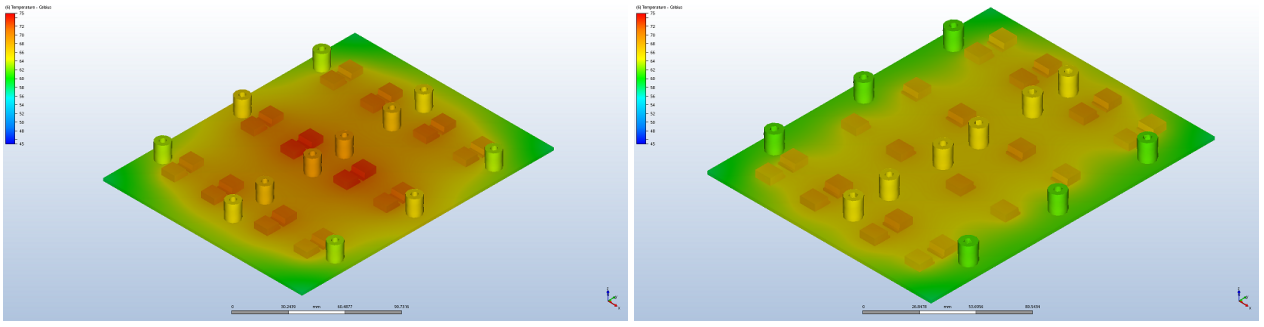


(a) Components in close proximity (Max temp: 87.516 °C).

(b) Good space distribution between components (Max temp: 73.776 °C).

Figure 4.10: MOSFET space distribution comparison simulation.

From Figure 4.10 it was identified that the MOSFETs on the outer edges of the PCB were cooler than those in the center. The PCB was remodeled to try rectify this, with the results seen in Figure 4.11 showing a reduction in temperature of 2.569 °C .



(a) Components placed in center (Max temp: 73.776 °C).

(b) Components placed towards the edges and away from the center (Max temp: 69.270 °C).

Figure 4.11: Simulation showing comparison of MOSFETs placed towards edges.

It is understood that there will be a thick aluminium base plate to distribute heat, and potentially solve the hot spot issues seen in figures 4.10 and 4.11. There is however a thermal resistance at the mating surfaces between the PCB and base plate. Additionally, there is a thermal resistance between the MOSFETs and the PCB core due to the dielectric used on the PCB. These thermal resistances will cause the hot spots shown in the simulations to still remain as can be seen in the following set of simulations.

The thermal conductivity of the TIM used is stated in the datasheet as 2.9 W/m· K, and the paste thickness is approximately 20 μm [41, 42]. Thus the thermal resistance is calculated

as

$$R_{\theta(paste)} = Paste\ Thickness \times \frac{1}{Thermal\ Conductivity} =$$

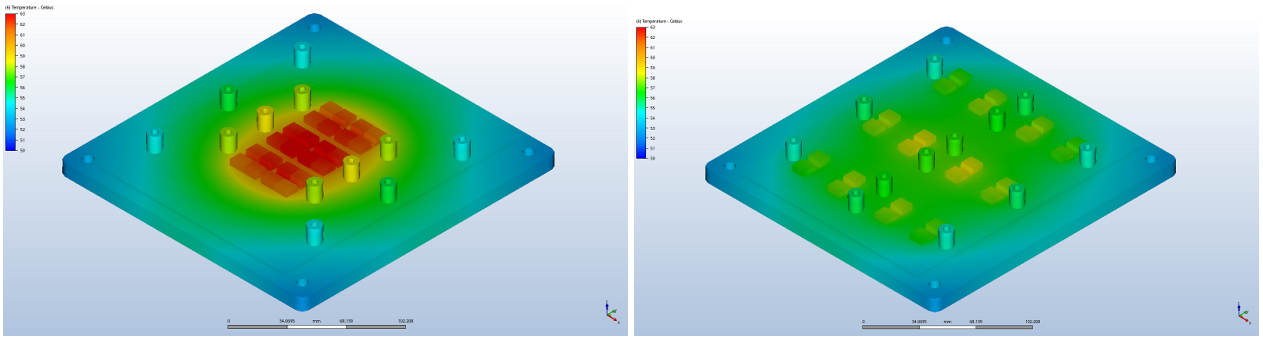
$$20\mu m \times \frac{1}{2.9} = 6.897\frac{K \cdot mm^2}{W}. \tag{4.2}$$

Likewise, knowing the thermal conductivity of the PCB dielectric is 1.5 W/m· K [43], the thermal resistance can be calculated as

$$R_{\theta(Dielectric)} = Dielectric\ Thickness \times \frac{1}{Thermal\ Conductivity} =$$

$$0.1mm \times \frac{1}{1.5} = 66.667\frac{K \cdot mm^2}{W}. \tag{4.3}$$

The simulation in Figure 4.10 was rerun with the aluminium base plate and additional thermal resistances to investigate their effects. The results of which can be seen in Figure 4.12 where there is still a notable difference of 4.95 °C.



(a) Components in close proximity (Max temp: 63.58 °C).

(b) Good space distribution between components (Max temp: 58.63 °C).

Figure 4.12: MOSFET simulation with 10 mm aluminium plate.

4.6 Selection of best switching component

The aim of this section is to analyze and compare the optimal PCB designs with the chosen switch options. From the results attained in this section the best switching component can finally be chosen, thus completing block 5 in Figure 2.1.

All of these simulations are run in the worst-case scenario of full power at standstill. Therefore, there is zero air movement resulting in only conduction cooling. The heatsink used in this simulation is an appropriate off the shelf heatsink. It is important to note that the heatsink is not the focus in this simulation, rather the max temperature for each switching component choice.

The same thermal interface material used between the PCB and 10mm aluminium plate in section 4.5 is used between the aluminium plate and the heatsink. A set of control factors were re-established to ensure valid results, these are:

- The ambient air temperature volume will be set to 1 m^3 allowing the temperature to converge to the boundary conditions

- The boundaries of the ambient air volume will be 40 °C
- The thermal interface material used between all mating surfaces has a thermal conductivity of 2.9 W/m· K
- The total heat generation power will be for a switching frequency of 50 kHz from Table 3.5
- The total heat generation power will be divided equally between all MOSFETs

In Figure 4.13 an example simulation for the BUK7626-100B can be seen.

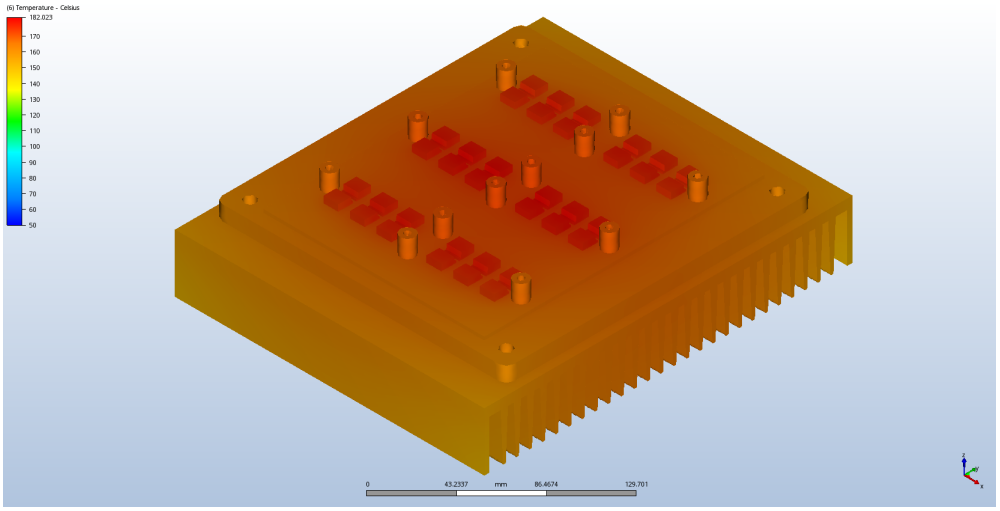


Figure 4.13: Motor drive temperature with Mellowcabs heatsink.

The maximum temperature reached for each MOSFET configuration can be seen in Table 4.3 below.

Table 4.3: Thermal comparison of MOSFET configurations sorted by maximum temperature.

Device	Max temperature(°C)	Total power(W)	Thermal resistance(°C/W)	Parallel MOSFETs
FQB44N10TM	226.41	691.34	1.03	4
BUK7626-100B	182.02	557.49	0.95	6
STB35NF10	175.42	567.98	1.30	8
CSD19506KTT	137.48	392.09	0.40	4
IPB083N10N3	133.10	390.69	1.20	12
CSD19535KTT	106.06	259.94	0.50	4
CSD19532KTT	92.45	211.50	0.60	6

From the results in Table 4.3, it can be seen that regardless of the number of devices or thermal resistance of the MOSFETs, the higher the losses the higher the maximum temperature. Additionally, it can also be seen that in order to use the FQB44N10TM, BUK7626-100B and STB35NF10 a better cooling solution would be required. From the results attained in chapter 3 as well as the results in Table 4.3 it is clear that the two best MOSFET options are the CSD19535KTT and CSD19532KTT.

Chapter 5

Hardware

5.1 Introduction

In this chapter, the decisions made during the hardware design of the example application PMSM drive are discussed. A key decision made at the beginning of the design process was to ensure full cross-compatibility with the current drive used by MellowCabs. To achieve this, the drive must meet a number of set requirements such as size and connector configuration. Designing the drive with this in mind is to ensure minimal effort in the process of testing through the use of their vehicles.

It was decided to design the drive with the power inverter module and control hardware module on two separate stackable PCB's. This decision was made due to key factors such as size restrictions and large heat dissipation requirements. As a consequence of this decision, the high current switching components could be separated from the sensitive control circuit thus, helping to reduce EMI related issues.

5.2 Literature related to hardware

5.2.1 Literature overview

The literature in this chapter begins by discussing and comparing solutions to the challenge of driving a MOSFET in switching operations. It then follows on to compare the different options available for current sensing. A brief overview of analog filters is covered as this is used in all the voltage and current measurements. Finally the switch node ringing phenomenon is discussed as well as possible ways to reduce this.

5.2.2 Driving MOSFETs

The first challenge which has to be overcome with driving a MOSFET is the charging and discharging of the internal MOSFET capacitances, as mentioned in section 3.2.5.2. The current required to charge or discharge these capacitances is supplied or sunk through the MOSFET driver. For this reason, when choosing a MOSFET driver it is important to ensure that the driver has a sufficient current rating to achieve the required switching speeds of the application.

Most switching power applications make use of a bridge configuration with a high and low side switch. By placing the switches in this configuration, complications can arise with regards to driving the switches. One of these complications is the inability of the control circuitry to drive the high side switches gate above its threshold voltage. This can be seen

with the example of a basic buck converter shown in Figure 5.1. For the voltage V_{M1} to be approximately zero V_{GS_1} of the switch must be kept above the gate threshold voltage V_{TH}. Thus, the gate voltage of $M1$ must be approximately equal to $V_d + V_{TH}$. This poses a large challenge for control schemes as typically their maximum output voltage is equal to or bellow V_d [44].

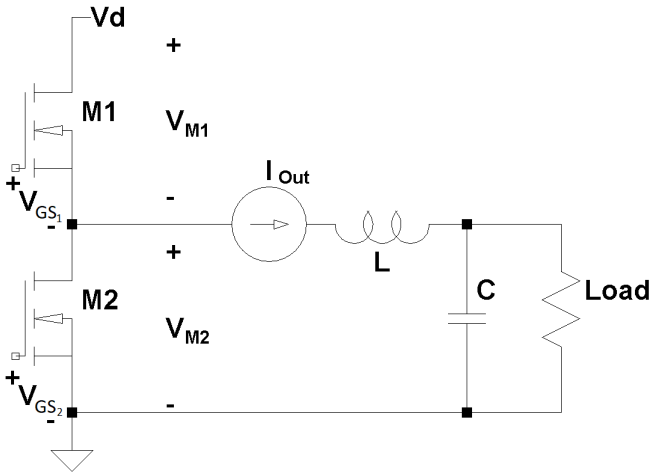


Figure 5.1: Simple buck converter circuit.

There are several methods of overcoming the challenge of high side N channel MOSFET driving. Typically these methods are split into the two categories of isolated and non-isolated. In applications where the supply voltage is greater than 24 V, it is often seen that a layer of isolation is implemented between the control circuitry and the MOSFET bridge. This allows for a number of MOSFET driving options, the first of which can be seen in Figure 5.2 [45]. The isolation layer in this solution is formed by the transformers placed between the driver and the MOSFET gates. The advantage of this solution is the uniformity between the high and low side gate driving circuits. However, it can be seen that after the transformers, additional circuitry is required, increasing cost and form factor size.

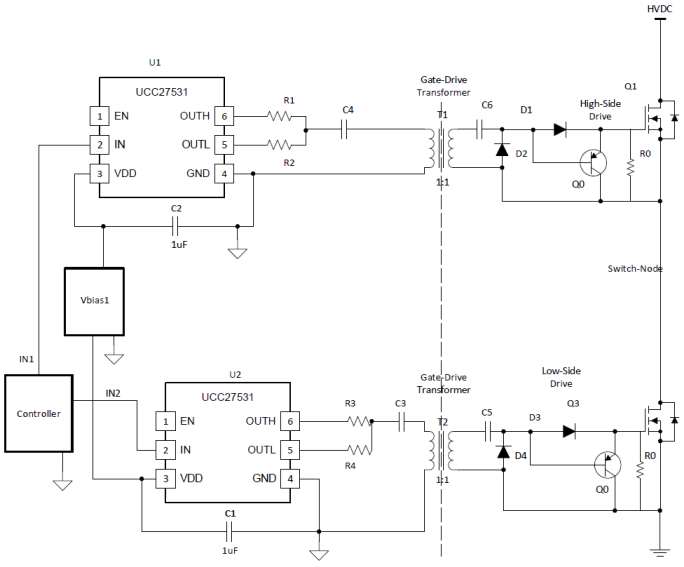


Figure 5.2: Transformer based gate driver circuit [3].

Another solution is to use an isolated power supply for the high side driver. An example of this solution can be seen in Figure 5.3. It is important to note that the ground reference of the high side gate driver is connected to the phase output [3]. This allows the supply voltage of the high side driver to rise above the input supply voltage. Additionally, the signal connections from the MCU to the high side driver are isolated due to the fact that the drivers ground reference will rise with the switching node. If the power ground reference for the output is the same as for the control circuitry, it is not strictly necessary for the low side signal connections to be isolated. However, isolation is typically added for protection in high current applications.

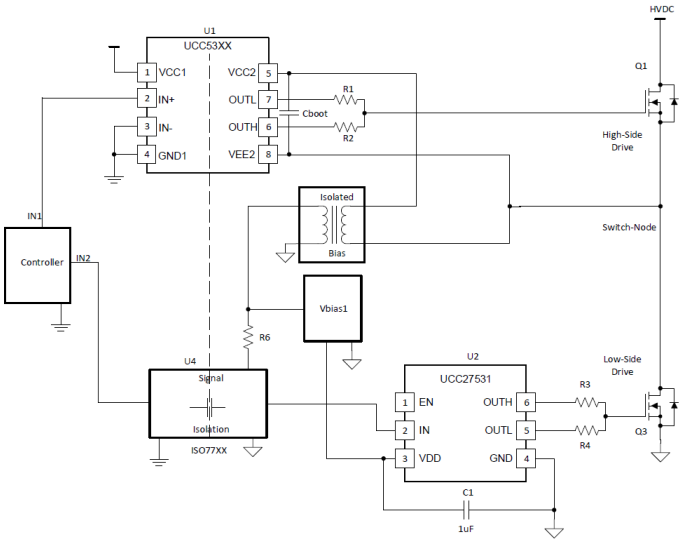


Figure 5.3: Bootstrap capacitor circuit with capacitive signal isolation [3].

The last solution covered in this section again uses a MOSFET gate driver which incorporates the isolated signal connections. This solution uses a bootstrap capacitor configuration, an example of which can be seen in Figure 5.4. It is clear that this solution has the least complexity and lowest component count thus, making it favourable.

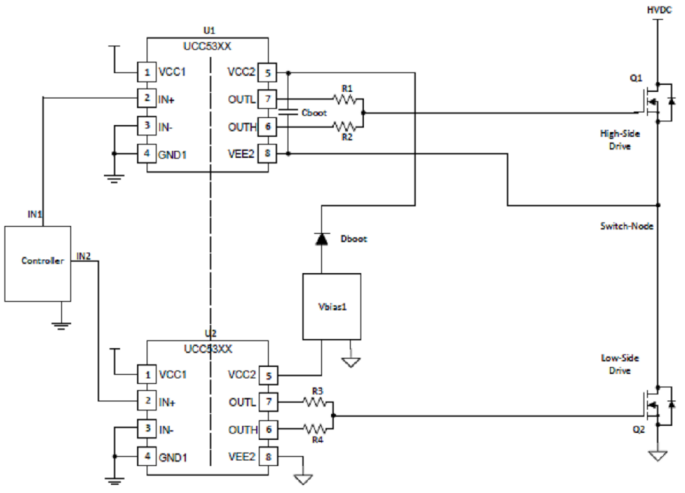


Figure 5.4: Bootstrap capacitor circuit with isolated gate drivers [3].

5.2.3 Current sensing

Current sensing is one of the most important elements to a PMSM drive, as it along with the rotor angle, is the only information required to implement FOC. Additionally, current sensing plays a vital role in the safety aspect of the drive by facilitating current limiting. Current limiting can prevent serious damage and even injuries in the case of an accidental short circuit.

There are three primary current measurement methods used in power electronics, these being:

- Transistor
- Resistor
- Magnetic

5.2.3.1 Transistor

Transistor datasheets for MOSFETs provide a value for the device's on state resistance. By measuring the voltage over this equivalent resistance the current through the device can be calculated. The advantage of this is that no additional components are needed in the current path, resulting in no additional losses. However, this method is very inaccurate due to the variance of $R_{DS(on)}$ with respect to temperature [46]. Figure 5.5 shows a graph of the $R_{DS(on)}$ vs temperature from the CSD19532KTT MOSFET datasheet. It is clearly seen that there is a variance in $R_{DS(on)}$ with temperature. Using a temperature sensor and the data from Figure 5.5, this can be compensated for. However, regardless of this there will still be inaccuracies due to the variance in $R_{DS(on)}$ between devices from manufacturing.

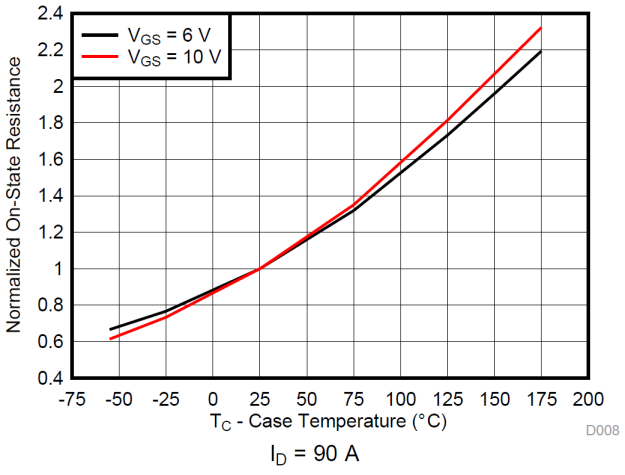


Figure 5.5: CSD19532KTT, $R_{DS(on)}$ vs temperature.

It is clear that this method is not accurate enough for the application of a PMSM motor drive. However, in an application such as a buck converter, where the aim is to only measure for over-current protection, this could be an ideal solution.

5.2.3.2 Resistor

Shunt resistors are a very commonly used method of sensing current due to their high accuracy combined with their low cost. To determine the current through the resistor, the voltage across the resistor is measured after which Ohm's law is used to calculate the current.

In the application of a three-phase inverter, there are typically three configurations for shunt resistor current measurement. These are low side, high side and inline measurement, which refers to the placement of the shunt resistor in the system.

Figure 5.6 shows an example of low side shunt resistor current sensing. The advantage of using a low side shunt resistor is the simplicity in the amplifier circuity required, as the voltage across the resistor is relative to ground. Having a voltage drop over the shunt resistors does however have the negative effect of shifting the ground reference of other circuity. Depending on the application this can cause large complexities due to the need for isolation [47].

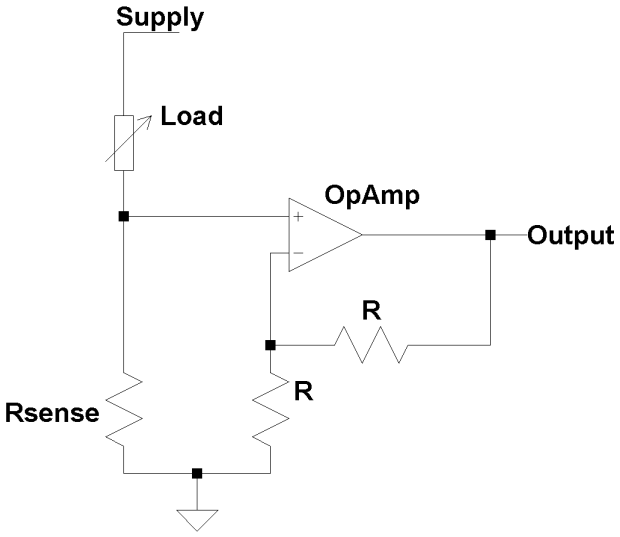


Figure 5.6: Low side shunt resistor.

High side current sensing solves the problem of a shifting ground reference, this is at the compromise of a much a more complex amplification circuit. An example of high side current sensing can be seen in Figure 5.7, where the differential amplifier can also be seen. Due to the shunt resistor being placed at the supply rail, the voltage levels are high thus, amplifiers with high voltage capabilities are required which can add a significant cost so the design [47].

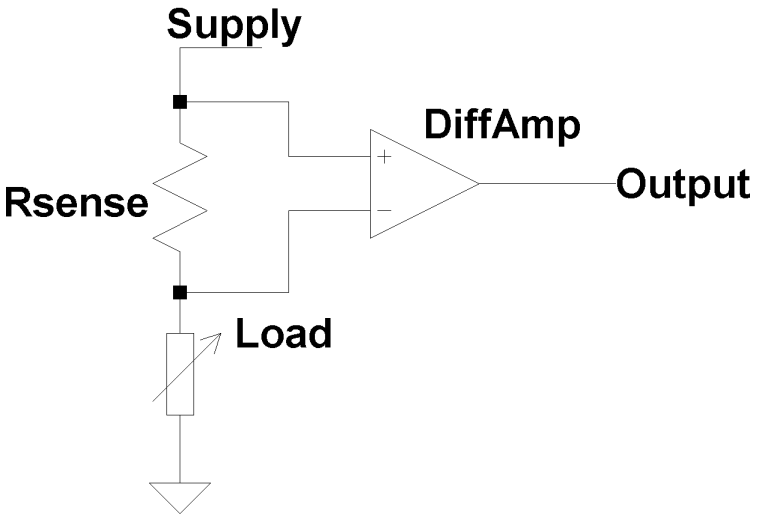


Figure 5.7: High side shunt resistor.

Inline current sensing using a shunt resistor, involves placing the resistor in series with the motor phases as seen in Figure 5.8. Although similar to the previously mentioned method, the distinct difference with this method is the lack of a constant voltage on either side of the resistor. Due to this as well as the placement of the resistors in the circuit, the input voltages to the amplifier vary at a high rate. This can lead to large common mode transients being passed through to the amplifier, resulting in a current reading error [48].

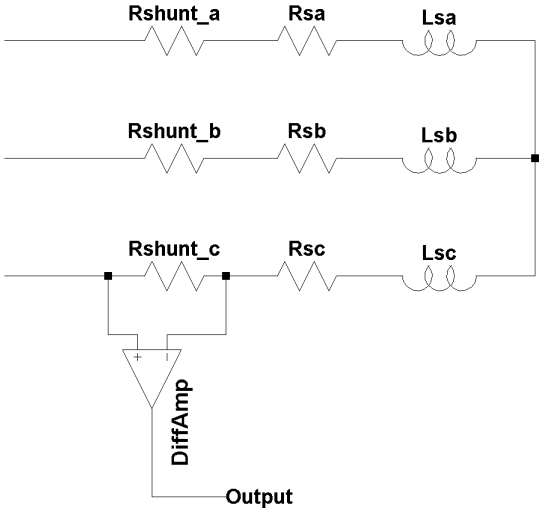


Figure 5.8: Inline shunt resistor.

5.2.3.3 Magnetic

The primary advantage of magnetic current sensing is the inherent isolation that is formed. The most common methods of magnetic current sensing is the Hall effect as well as current transformers and the Rogowski Coil.

A current transformer is considered a lossless current sensing solution due to the fact that the current can pass through the primary windings with very little losses. The main advantage of a current transformer is the ability to scale the output of the transformer by adjusting the turns ratio on the secondary side. The disadvantage of a current transformer is the

requirement for an alternating current to create a change in flux. However, in most motor drive applications this is not an issue [46].

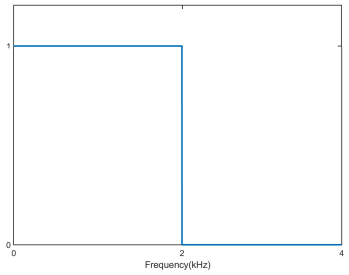
The Rogowski coil works on a very similar principle to the current transformer, with the difference of not needing a core with high permeability. The Rogowski coil also relies on Faraday's law of "the total electromotive force induced in a closed circuit is proportional to the time rate of change of the total magnetic flux linking the circuit". Due to the Rogowski coil containing an air core, it is more suited in many applications such as measuring current in complex spaces. This results in the Rogowski coil primarily been used in temporary applications [49].

When a wire conducting current is placed in a perpendicular magnetic field, a voltage is induced which is known as the Hall effect. This is used within Hall effect current sensors which can be of either the open or closed-loop configuration. Closed-loop Hall effect sensors typically result in higher accuracy over a larger current range. The advantage of the Hall effect current sensor is that they can very easily be integrated into a design compared to the other magnetic currents sensing options. However, Hall effect sensors are typically expensive and can have a fluctuation in accuracy, depending on the temperature as well as having limited bandwidth [49, 50].

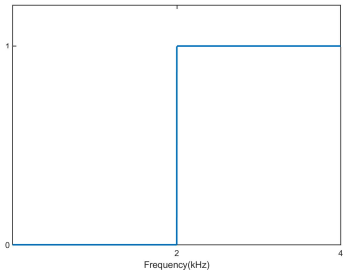
5.2.4 Analog filters

Analog filters are a circuit in which the characteristics of an electronic signal is altered with regards to the frequency. There are two main forms of analog filters these being passive and active filters. A passive filter requires no external power source and relies on only the signal being filtered. Whereas, an active filter uses a component such as an operational amplifier, which requires an external power source. The key advantages of using active filters is the ability to buffer the filter from the input signal. Additionally, active filters typically do not require inductors which are highly susceptible to noise. This study will focus primarily on the active filter due to its use in the hardware design of the VSD [51].

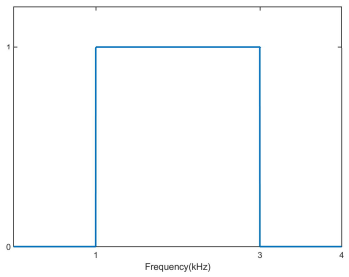
Depending on the requirements of the filter by the system, a topology of either low-pass, high pass, band-pass or band-stop filter will be designed. The ideal frequency response of each of the mentioned typologies can be seen in Figure 5.9, where it is key to note the low-pass filter as this will be focused on in more detail.



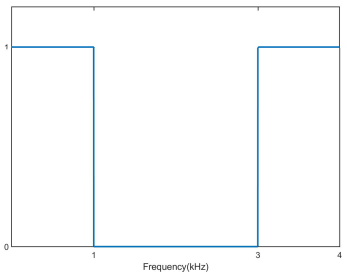
(a) Low-pass filter.



(b) High-pass filter.



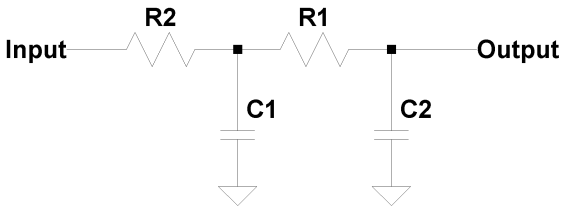
(c) Band-pass filter.



(d) Band-stop filter.

Figure 5.9: Filter topology frequency responses.

Figure 5.10a shows a passive second-order low-pass filter which is formed by a two-stage RC circuit. The gain of this circuit has a maximum of $\frac{1}{2}$ thus, to solve this, in 1955 R.P Sallen and E.L Key formulated the circuit in Figure 5.10b [52]. From this, it can be seen that there is a unity gain operational amplifier with capacitor C2 not connected to ground, but instead the output of the operational amplifier. This forms a feedback loop and the common filter circuit known as the Sallen-Key architecture [53].



(a) Second-order passive filter.

(b) Sallen-Key second-order filter.

Figure 5.10: Second-order low-pass filters.

5.2.5 Switch node voltage ringing

An example of Switch node voltage ringing can be seen at the rising and falling edges of the pulse in Figure 5.11. This can cause damage to components if the voltage overshoot rises above maximum component ratings. Additionally, this high-frequency ringing can cause a high level of electromagnetic noise.

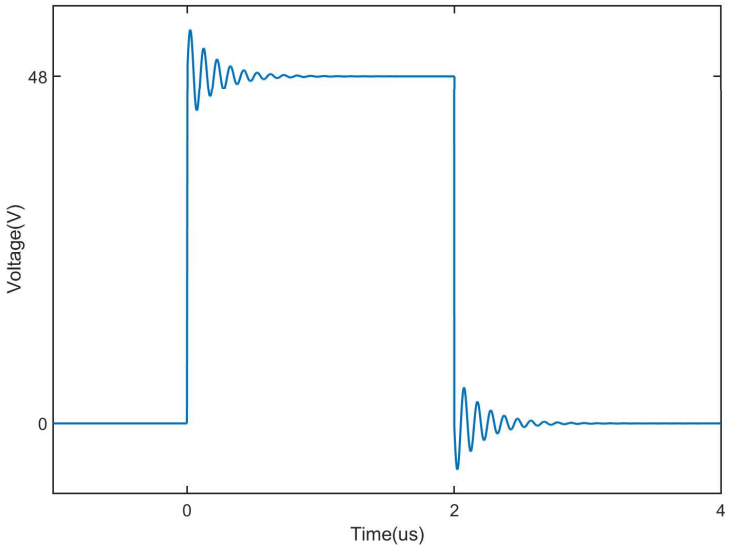


Figure 5.11: Switch node voltage ringing example.

Switch node ringing is caused by the parasitic components seen in Figure 5.12, where the parasitic components are within the red blocks. When switch M1 is off and switch M2 is on, current flows from the source of M2 to the drain. Thus, when the deadtime period is now entered and switch M2 is turned off the current through M2's parasitic inductors must continue to flow, thus conduction takes place through the MOSFET body diode. After M1 is turned off the energy stored in M1's parasitic inductance is discharged by raising the switch node voltage above the supply voltage. Once this energy is dissipated, the drain to source capacitor of M1 must now be charged to the switch node voltage. This repetitive process is caused by the LC tank circuit, and causes the ringing [54].

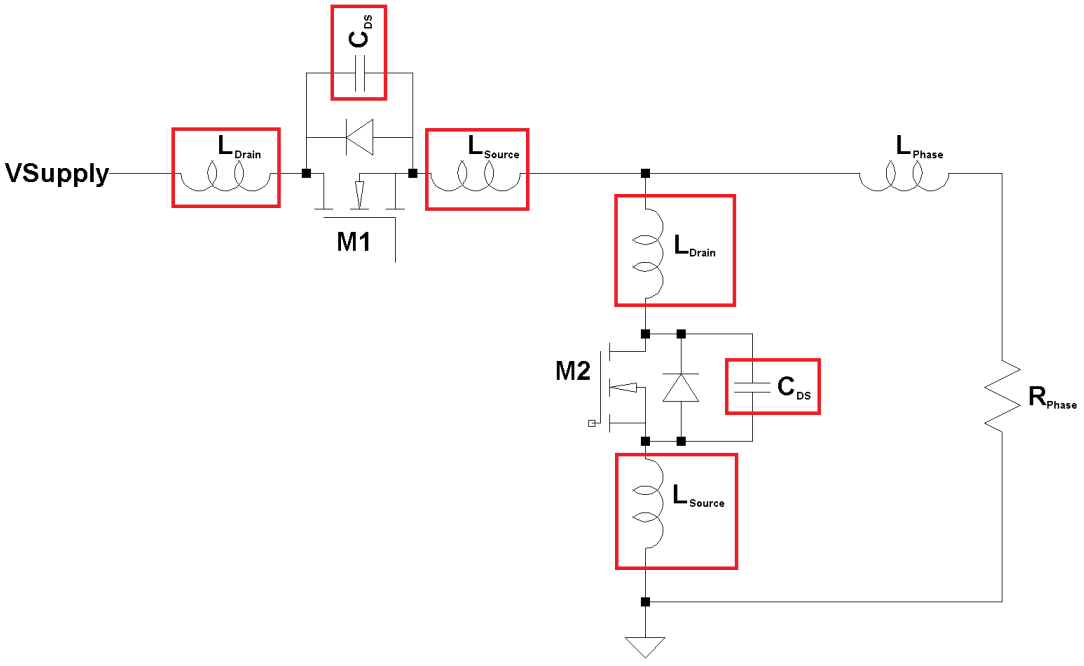


Figure 5.12: Switch node voltage ringing parasitic components.

5.3 Hardware identification

5.3.1 Section overview

In this section, block 7 in the flow diagram shown in Figure 2.1 is completed by discussing each control hardware element. Through this discussion the requirements for each hardware element are determined.

5.3.2 Current sensors

In section 5.2.3 the different options for current sensing are discussed in detail. From this it can be seen that the transistor method is ideal for use in applications where accuracy is not very important. Thus, this is not a viable option to be used in a PMSM drive. Although the resistor method is a very commonly used method, with relative simplicity, it poses a number of issues. These issues tend to become difficult to overcome when measuring large currents and are primarily focused around the voltage drop over the resistor. These issues are typically solved through the placement of the resistor and the corresponding amplifier stage. However, this presents additional issues due to the relatively high supply voltage, as discussed in further detail in section 5.2.3.2. There is, however a third option of using the magnetic fields created from current flowing through a conductor. This can be achieved by making use of one of three common methods discussed in section 5.2.3.3. Of these three methods the hall effect sensing option was chosen for the design of the VSD. More detail on the actual design used in the VSD application can be seen in section 5.4.2.

5.3.3 Voltage regulation

In the PMSM drive design there are 3 voltage levels required, these being 13.5 V, 5 V and 3.3 V. Knowing the input voltage, output voltage and output current, the decision between a linear regulator or a switching regulator can be made. A more detailed discussion on the operation of linear and switching regulators can be seen in section **??**. This is used to aid in the calculations and decisions made in section 5.4.3.

5.3.4 Microcontroller

When choosing a MCU for the PMSM drive the primary focus is placed on the external peripheral needs, these being:

- A minimum of 12 ADC inputs
- 18 GPIO pins
- 12 PWM channels
- 1 CAN bus channel

Following the MCU peripheral requirements the focus is then placed on the clock speed to ensure sufficient calculation speed of the control loop. An added requirement for the MCU is that it must be possible to synchronise the PWM outputs. This is on the grounds that each of the six inverter switches are made up of two parallel MOSFET drivers. Thus, if they are not synchronised it could result in a short circuit between the positive supply and ground.

5.3.5 MOSFET drivers

Due to the aim of the MOSFET driver being to supply the MOSFET gates with sufficient current to charge the gate capacitance within a sufficient time. The focus is placed on the maximum supply and sink current when choosing a MOSFET driver. Following this the focus is placed on ensuring the maximum voltage ratings of the drivers are not exceeded. Additionally, it is important for the MOSFET drivers to add a layer of isolation between the PMSM and the MCU as is further discussed in section 5.2.2.

5.4 Circuit design and layout

5.4.1 Section overview

In this section the schematic design as well as the PCB layout for both the upper and lower PCBs will be discussed. This completes section 8, in Figure 2.1 discussed in chapter 2.

5.4.2 Lower PCB

The lower PCB of the VSD is comprised of three main sections, all of which are related to higher currents. These sections are the MOSFET switches, supporting MOSFET gate drivers and finally the current sensing. Due to the high currents, the decision was made to use aluminium as the substrate for this PCB. Using aluminium as the PCB's substrate allows for surface-mount MOSFETs to be used. This decreases the required space needed for the MOSFETs whilst maintaining efficient heat dissipation. Additionally, the aluminium core PCB allows for higher currents to safely be carried through the PCB traces. However, due to the heat transfer capabilities of the aluminium PCB, all components had to be baked onto the PCB for soldering to be possible.

The final PCB design for the lower board can be seen below in Figure 5.13. It is important to note the unconnected nodes. These nodes are connected via the upper PCB allowing more area for the current carrying copper pours.

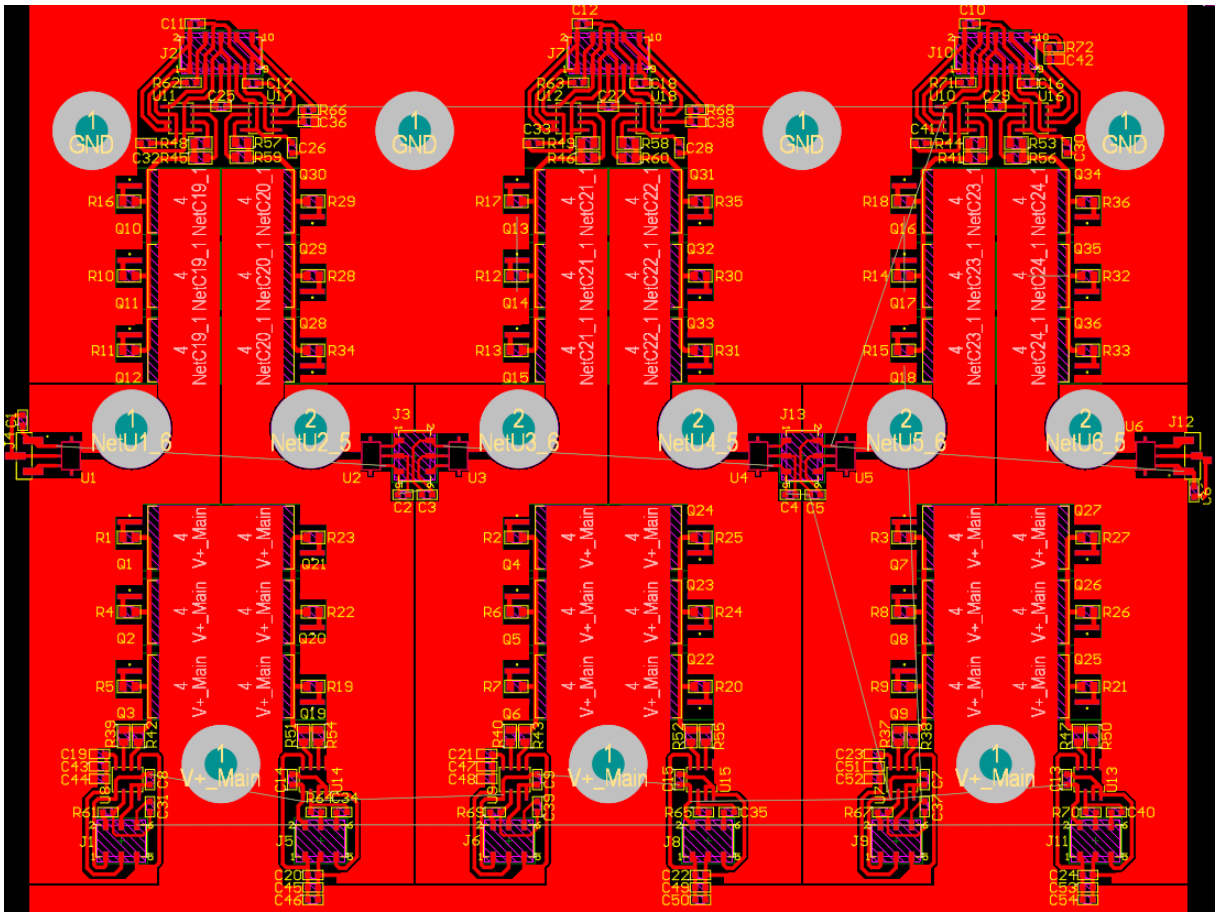


Figure 5.13: Lower PCB design (Not to scale).

Current sensors

There are a number of different options of Hall effect current sensors, of which the $ACS780KLRTR-150B-T$ from Allegro MicroSystems was chosen. This is due to its bidirectional current capabilities of ± 150 A, and its surface-mount package. The $ACS780KLRTR-150B-T$ has an analog voltage output with a value of 13.33 mV/A with a DC offset of $\frac{1}{2}$ Vcc to accommodate the negative current capabilities.

Although the $ACS780KLRTR-150B-T$ has a very high current handling capability, from section 3.3 it is known that a minimum of 220 A peak current per phase is required. Consequently due to all six MOSFETs being placed in parallel. It was decided to place two current sensors in parallel, separating the parallel MOSFETs into two sets of three. As a result of component placement constraints, the sensors were placed as seen in Figure 5.14 where the current sensors can be seen in the green blocks. The green arrows in Figure 5.14 indicate the direction of positive current flow. From this it can be seen that they are opposite in polarity relative to the actual positive flow of current shown in blue.

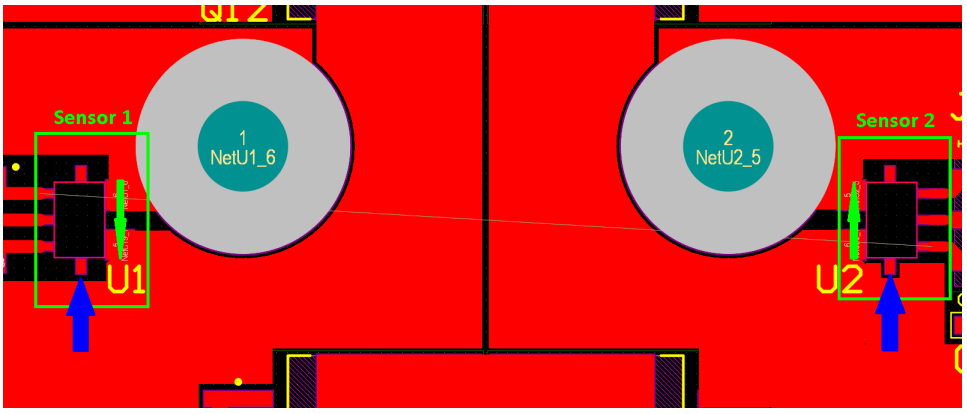


Figure 5.14: Current sensors in parallel.

To solve this problem, as well as add the current sensor outputs together a simple analog circuit can be used. This would be achieved by removing the $\frac{1}{2}$ Vcc offset from both sensors, after which one of them would be inverted before they are both added. However, this same process can be achieved computationally by the MCU, with the added benefit of a reduction in components and cost. Furthermore, it is possible to monitor the currents from each sensor to identify a MOSFET fault. If this is detected, the faulty MOSFETs can be disabled to allow the vehicle to return in a "limp-home" mode.

The output of the current sensor with the DC component removed can be seen in Figure 5.15. It can be seen that the high rate of change in switching currents due to switch node voltage ringing is inducing a large amount of noise on the signal.

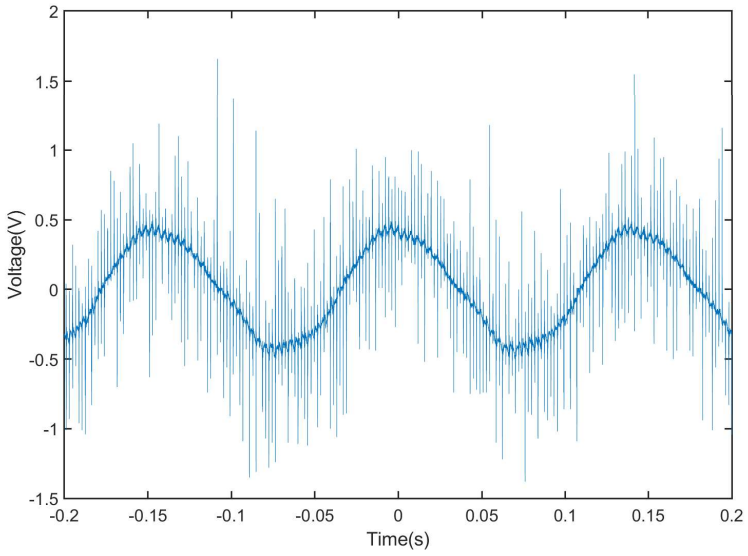


Figure 5.15: Current sensors output.

To test the accuracy of the current sensors, the measured sensor outputs are passed through a moving average filter to remove the high-frequency noise. The voltage is then converted to current using

$$I_{sense} = \frac{V_{sense}}{13.333 \times 10^{-3}}. \tag{5.1}$$

I_{sense} is then multiplied by two due to the fact that each current sensor carries half the total phase current. This is then compared with measurements taken using the Tektronix TCP303 current probe which can be seen in Figure 5.16.

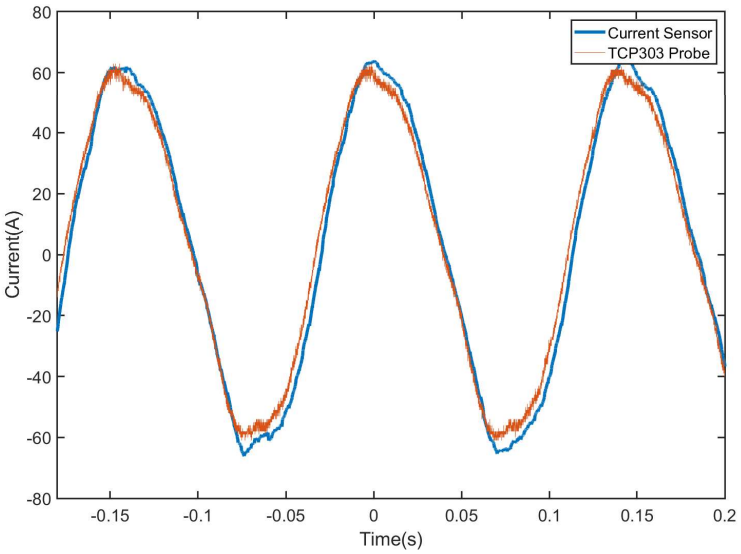


Figure 5.16: Current measurements vs time.

From this, it can be concluded that if the noise is removed, the current sensor accuracy is sufficient for this application. Additionally, through a calibration process in production. The accuracy can be further improved with compensation by the MCU.

MOSFETs

Simulations were conducted in chapters 3 and 4 to determine the best MOSFET to use for both efficiency and thermal reliability. This is used to determine the form factor of the lower PCB as the number of MOSFETs required would primarily determine the size. It was decided to place six MOSFETs in parallel thus allowing for both four CSD19535KTT and six CSD19532KTT to be tested. Additionally, six CSD19535KTT MOSFETs could be placed in parallel, thus allowing the PMSM drive to be tested at higher power levels. Knowing that two current sensors had to be used in parallel, the MOSFETs were required to be placed in two sets of three in parallel.

In chapter 4, the MOSFET placement was already designed to optimise heat distribution. Therefore, the majority of the design decisions related to the MOSFETs were ensuring the traces around them were sufficient to carry the currents required. It was soon identified that the supply and ground traces were not going to be sufficient in the restricted lower PCB size. To solve this, aluminium bus bars were added to the top of the power element bushes as seen in Figure 5.17.

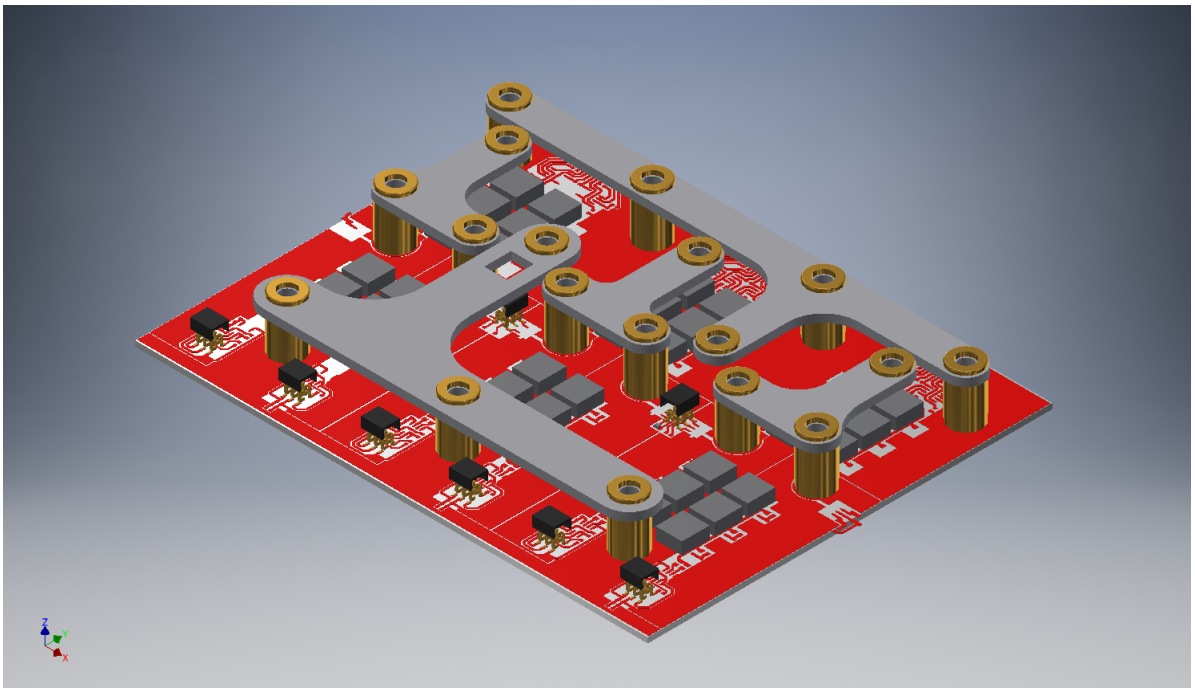


Figure 5.17: Drive with bus bars.

MOSFET drivers

The method of MOSFET driver chosen for the design of this inverter is shown in Figure 5.4. Therefore the UCC5390SC by Texas Instruments was chosen as this contains the internal signal isolation with the ability to supply or sink a maximum of 10 A. The value of the boot capacitor is found by

$$C = \frac{Q_{Gtot}}{V_{Cdrop}} = \frac{75 \times 10^{-9} \cdot 3}{13.5 \times 0.03} = 555.6nF \tag{5.2}$$

where C is the capacitance needed, Q_{Gtot} is the total gate charge the driver has to supply and V_{Cdrop} is the maximum voltage drop of the capacitor. Q_{Gtot} is calculated as the total gate charge of one MOSFET multiplied by three due to three MOSFETs being in parallel. The maximum voltage drop is calculated as three percent of the MOSFET supply voltage which is 13.5 V. From 5.2, it was decided to rather use two 330 nF capacitors in parallel instead of one capacitor to reduce the ESR of the boot capacitor.

A 10 Ω resistor was placed on the V_{OUTH} and V_{OUTL} pins of the MOSFET driver. This in conjunction with the 5.1 Ω resistors placed at the gate of each MOSFET limits the current supplied or sunk by the driver.

To calculate the minimum reverse bias voltage the boot diode must be able to withstand the circuit in Figure 5.18 is used where V_{IN} is 56 V.

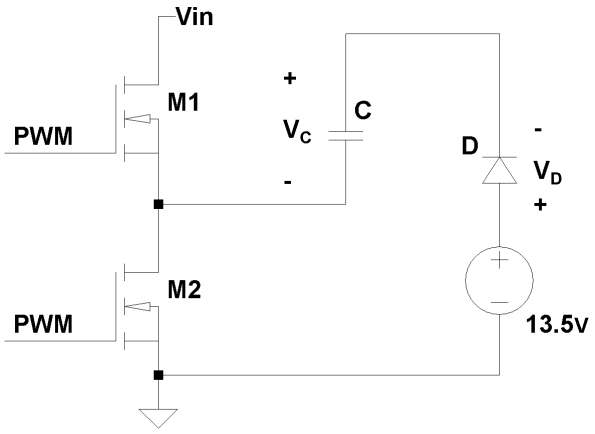


Figure 5.18: Boot capacitor circuit with diode.

When switch M1 is on, the voltage V_C is calculated as

$$V_C = V_1 = 13.5 - V_D = 13.5 - V_\gamma \tag{5.3}$$

where V_γ is the forward voltage of the diode. When switch M1 is turned off and switch M2 is turned on, V_C remains the same due to the properties of a capacitor. From this, the voltage over the diode can then be calculated as

$$V_D = 13.5 - V_C - 56 = 13.5 - 13.5 + V_\gamma - 56 = V_\gamma - 56. \tag{5.4}$$

Thus the minimum reverse voltage of the diode that can be chosen is 60 V. Figure 5.19 shows the reverse voltage measured across the diode with a supply voltage of 24 V. It can clearly be seen that the transient voltages from switching cause the reverse voltage to be well above 24 V at maximum. Therefore, diodes with a reverse voltage of 100 V are recommended due to potential transient voltages.

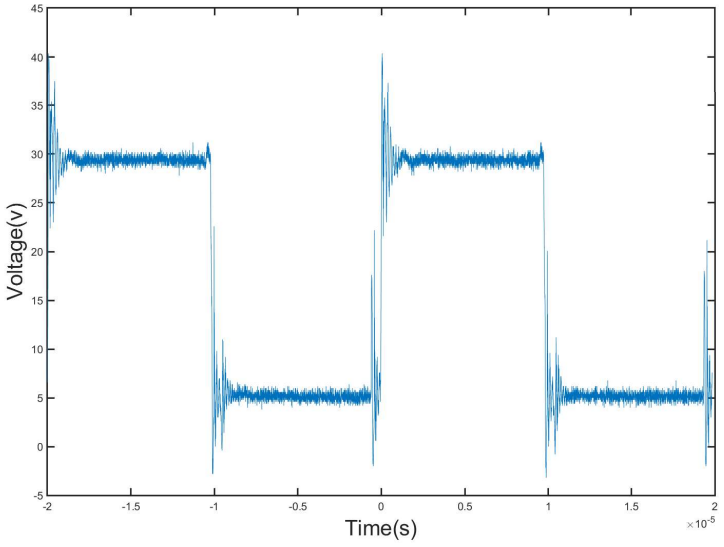


Figure 5.19: Voltage across boot capacitor diode.

As recommended by the MOSFET drivers datasheet, a filter was added at the signal input of each driver. This is to reduce the effects of potential noise induced between the MCU

and the gate drivers. The RC low-pass filter circuit was placed close to the signal pin on the driver, with values of $R = 100\ \Omega$ and $C = 33$ pF as recommended by the datasheet. This filter has a cutoff frequency of approximately 48 MHz, thus being high enough to have no shaping effect on the input signal to the driver as mentioned in the datasheet.

5.4.3 Upper PCB

The upper PCB consists of the supply bus capacitors as well as all the low current circuity such as filters, communications and the MCU. The upper PCB is divided into an upper and lower section, these being determined by the ground plane. The upper section is focused on the bulk capacitance used to reduce voltage ripple on the supply bus. Thus, the ground plane in this section is the supply ground. The lower section is focused on the MCU and the supporting circuity for controlling the VSD. Due to the communications ground reference possibly being of a different potential than the power ground as a result of voltage drop over the supply cable, a layer of isolation is added between the MCU ground and the supply ground. The horizontal center of the PCB is focused on filtering the phase voltages and currents. This design decision was made to keep the trace lengths of the analog circuitry as short as possible to reduce induced noise. The second key design decision was the placement of the 35 pin AMPSEAL automotive connector, due to its size and number of required trace connections. Thirdly the MCU was placed in the lower right corner and the 3.3 V regulator in the center. Additionally, the 13.5 V and 5 V regulators were placed on the left hand side of the board. Although it is not ideal for the regulators to be some distance from the MCU and control circuitry, they are placed as close as possible with extra capacitive filtering added to the supply line to eliminate noise.

The final upper PCB design can be seen in Figure 5.20 below. It is important to note that some nodes are not connected as this connection will be made via the bus bars or lower board.

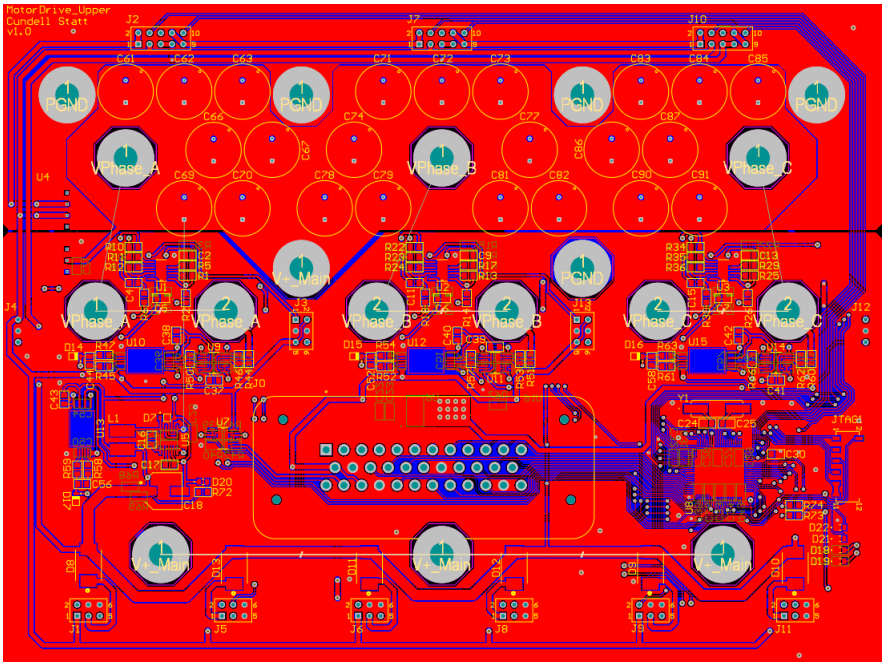


Figure 5.20: Lower PCB design (Not to scale).

Voltage regulation

Three separate voltages are required by the circuity in the PMSM drive, these being 13.5 V, 5 V and 3.3 V. The 13.5 V supply is exclusively supplying the MOSFET drivers and thus, unlike the other two supplies, does not need to be isolated from the supply rails.

*Non-isolated supply The 13.5 V non-isolated regulator only provides power to the MOSFET drivers. Therefore, calculating the minimum current the regulator must be able to supply is relatively easy with

$$I = \frac{Q}{t} = \frac{Q_{gate} \cdot N \cdot f_{sw}}{1} = \frac{75 \times 10^{-9} \cdot 36 \cdot 100 \times 10^{3}}{1} = 0.27\ A \tag{5.5}$$

where Q_{gate} is the total gate charge of one MOSFET, N is the number of MOSFETs and f_{sw} is the maximum switching frequency.

From this, the design decision between a linear or switching regulator can be made. This decision is based on the efficiency of the regulator, the temperature of the regulator and finally the cost. If a linear regulator such as the LM317HV is used, the efficiency of the regulator can be calculated as

$$eff = \frac{P_{out}}{P_{in}} \times 100 = \frac{13.5 \cdot 0.27}{56 \cdot 0.27} \times 100 = 24.1\%. \tag{5.6}$$

This is extremely low and thus a high temperature is expected. This can be calculated as

$$T_{junction} = T_{amb} + P_{loss} \cdot R_{\theta j-a} = 40 + (V_{in} - V_{out}) \cdot I \cdot 23 = 40 + (56 - 13.5) \cdot 0.27 \cdot 23 = 303.925°C. \tag{5.7}$$

From this, it is clear that it is not possible to use a linear regulator regardless of the cost savings. Thus, the MAX5035 from Maxim integrated was used with the circuit seen below in Figure 5.21. The inductor and capacitor values were calculated to result in a current ripple of less than 30% and a voltage ripple of less than 5%.

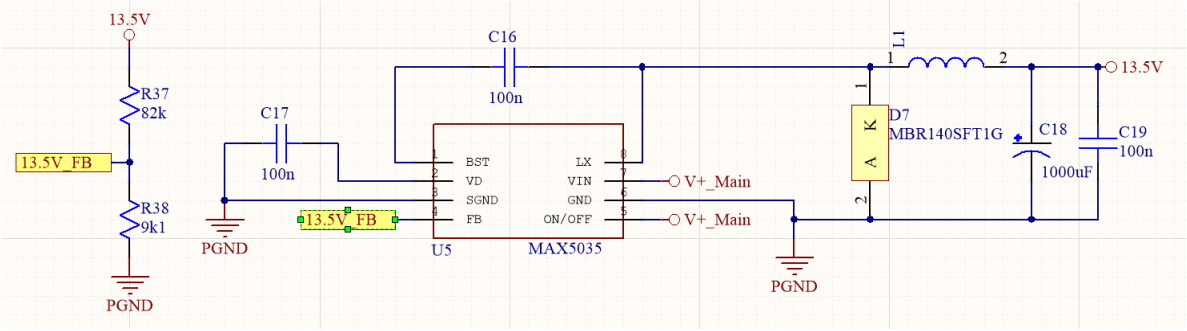


Figure 5.21: MAX5035 regulator circuit.

Isolated supply

For the isolated supplies it was decided that a complete DC-DC single output converter would be the best solution. This is due to the minimal space required compared to a custom isolated supply design. The converter chosen is the SPB05C-05 by Mean Well Enterprises which is capable of supplying a maximum current of 1000 mA. To create an isolated 3.3 V a linear regulator was placed on the already isolated 5 V supply as this was the most cost-effective solution. This can be done due to the MCU being the only component requiring 3.3 V thus the current demands are very low.

Phase voltage measurement

It is required that the phase voltages are filtered to remove the 50 kHz switching signal. Thus a simple Sallen-Key filter is to be implemented. To achieve this the MCP6H02 operational amplifier from Microchip is used. The maximum input voltage of the MCP6H02 is 16 V, thus the phase voltage of up to 56 V is reduced with a resistive divider using R44 and R46, as seen in Figure 5.22. After the voltage has been reduced the signal is fed into the second-order Sallen-Key low-pass filter. This is designed with a cutoff frequency of 1kHz, approximately one decade above the commutation frequency of the machine.

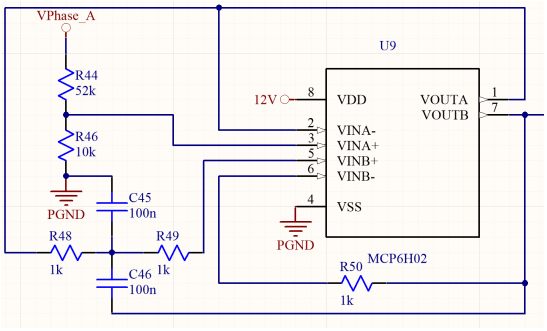


Figure 5.22: Sallen-Key filter for phase voltage measurement.

As a result of the isolation layer between the power ground and the MCU ground, the output of the Sallen-Key filter cannot be fed directly into the MCU's ADC. Thus, the isolation amplifier ISO224 by Texas Instruments is used. This isolation amplifier has a single-ended input range of ±12 V with a differential output of ±4 V. The relation between the input and output can be seen in Figure 5.23.From Figure 5.23 it can be seen that V_{OUTN} ranges between 2.5 V and 0 V for input values of 0 V to 15 V . Therefor, this signal can be fed directly into the MCU's ADC which has a range of 0 V to 3.3 V.

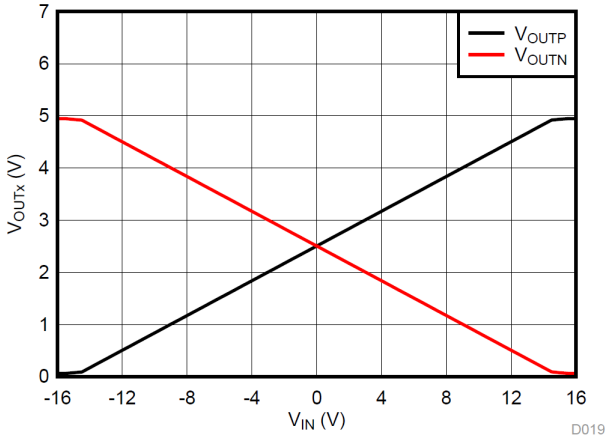


Figure 5.23: ISO224 output vs input [4].

From Figure 5.23 the relation between the input and output of OUTN is be calculated as

$$V_{in} = (V_{out} - 2.5) \times \frac{-15}{2.5} = (V_{out} - 2.5) \times -6. \tag{5.8}$$

Phase current measurement

One of the motivations for using the Hall effect current sensor is that it is inherently isolated from the signal it is measuring. Thus, the current measurement signal does not have to be isolated and is fed directly from the Sallen-Key low-pass filter into the MCU. This does however mean that the output voltage from the Hall effect sensors has to be scaled from a maximum of 5 V to 3.3 V. The voltage scaling, as well as the Sallen-Key filter for both current sensors of phase A, can be seen in the circuit shown in Figure 5.24.

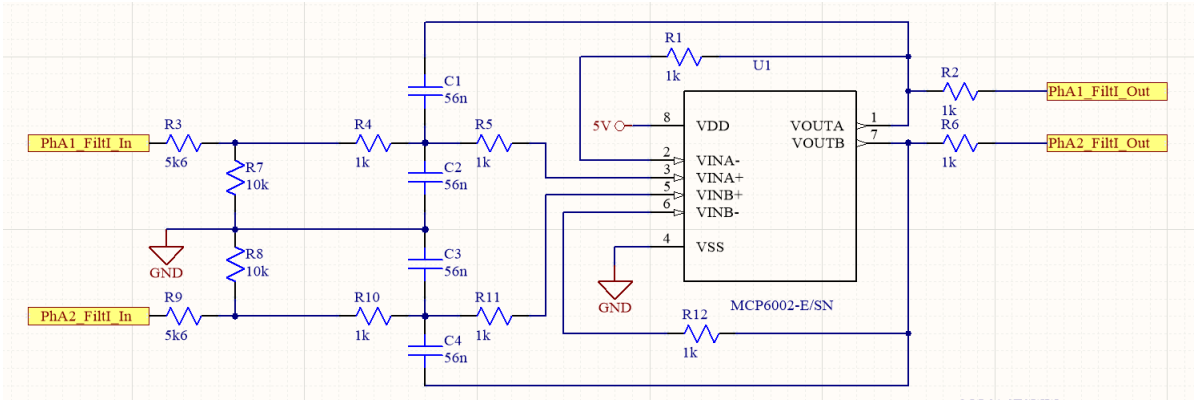


Figure 5.24: Voltage scaling and Sallen-Key filter circuit.

5.5 Microcontroller

A number of MCU options are available from different manufacturers such as Renesas, Microchip and Texas Instruments. However, due to the development resources available along with the affordability of Texas Instrument's C2000 series, the TMS320F28035 was chosen.

The 80 pin TMS320F28035 was chosen as it comes with fourteen ePWM outputs which can be selectively synchronised. Adittionally, it has sixteen 12-bit ADC channels which result in a 805.86 μV resolution and an enhanced CAN module. The TMS320F28035 has a maximum clock speed of 60 MHz, which will allow for calculations such as the Clarke and Park transforms to be performed at a sufficient rate.

It is important to note during the development process that the ePWM outputs are arranged into seven separate channels. This is done to allow each of the channel's two pins to be configured as a complimentary pair. Additionally, Deadband between these two outputs can be configured in the MCU's ePWM hardware module. This removes the need for Deadband to be added into the firmware's control algorithm.

5.5.1 External inputs

One of the requirements in the design of the PMSM drive is the cross-compatibility between it and the existing Mellowcabs BLDC drive. Therefore, the 35 pin AMPSEAL connector has to be used. This connector allows external inputs to be interfaced with the PMSM drive. These inputs along with their type are listed in Table 5.1 below.

Table 5.1: 35 pin AMPSEAL connector pin layout.

Pin Number	Name	Type
6	CANH	Digital InputOutput
7	CANL	Digital InputOutput
8	KSI	Digital Input
10	ACE128 pin 1	Digital Input
11	ACE128 pin 2	Digital Input
12	ACE128 pin 3	Digital Input
13	5V	Supply
14	GND	Supply
15	Hall-U	Digital Input
16	Hall-V	Digital Input
17	Hall-W	Digital Input
19	GND	Supply
20	ACE128 pin 4	Digital Input
21	ACE128 pin 5	Digital Input
22	ACE128 pin 6	Digital Input
23	ACE128 pin 7	Digital Input
24	Throttle Pot Wiper	Analog Input
25	Throttle 0-5V	Analog Input
26	5V	Supply
27	GND	Supply
28	Motor-Temp	Digital Input
30	Forward	Digital Input
31	Reverse	Digital Input
33	EMR	Digital Input
34	GND	Digital Input
35	Interlock	Digital Input

CAN bus is a communication standard designed to allow multiple devices to communicate with each other. It operates with a physical layer of two complementary connections thus, there is a CAN high line and a CAN low line.

The Key switch input (KSI) is an input to the PMSM drive to allow a level of security to be added to the system. The KSI input along with all the other digital inputs are designed with pull up resistors and thus, to input an "on" state they must be tied to ground.

The ACE128 rotary encoder is a device that uses eight pins to output the shaft angle to an accuracy of $\frac{360}{128} = 2.8125$ °. This is done by having one ground reference and seven outputs that get tied to ground to represent a 0 and left open to represent a 1. This device is intended to be used for development purposes only, however the digital input pins will remain for possible uses in a production scenario.

There are two different analog options to supply a throttle input to the drive. The first is a voltage supply between 0 V and 5 V, where 5 V is full throttle. The second uses the same principle but supplies a voltage through the use of a variable resistor with 0 V and 5 V also applied to it. Although the second option is seemingly redundant, it is added to maintain the cross-compatibility as the existing drive has this connection.

The Motor temp input is simply a thermostat within the PMSM allowing the drive to be

notified of an over-temperature within the PMSM. This can be used to either place the drive in a limp-home mode by reducing the power level supplied to the PMSM. Or it can be used to completely disable the PMSM.

The forward and reverse operate simply to determine the direction in which the PMSM rotates. These signals can also be used to place the PMSM in free-spin or breaked mode by applying the signals in truth Table 5.2 below.

Table 5.2: Forward and reverse truth table.

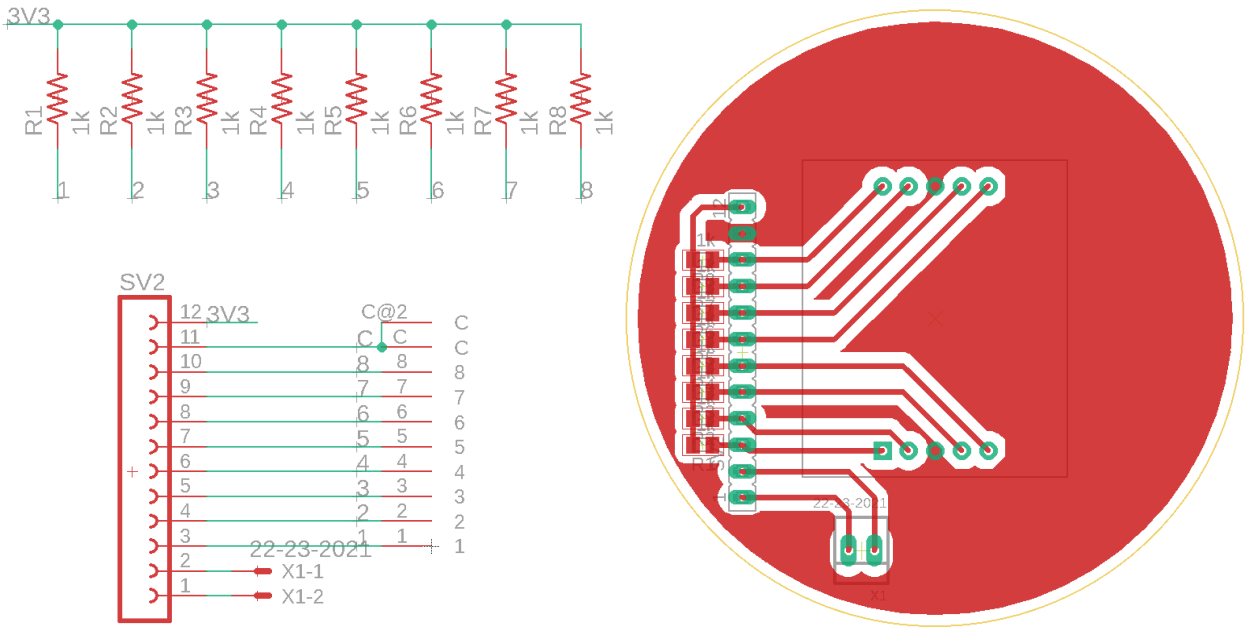
Mode	Forward	Reverse
Forward	1	0
Reverse	0	1
Free spin	0	0
Breaked	1	1

The emergency reverse switch (EMR) immediately reverses the direction of rotation on the input of the switch being tied to ground. This typically works along-side the Interlock switch which is an emergency stop signal.

5.6 Rotor shaft sensor

The 5 kW PMSM is fitted with a rotor angle sensor that uses three Hall effect sensors. Each of which outputs six changes of state through one full mechanical rotation. Therefore, there is a total of 18 state changes between all three sensors for one full mechanical rotation, resulting in a 20° resolution. However, due to the PMSM containing three pole pairs there are three electrical rotations for each mechanical rotation resulting in a 60°resolution. With this resolution, the machine can only be controlled using trapezoidal control if sensor-less control is not implemented. For this reason, it was decided to fit a more accurate rotor angle sensor for the initial development of the drive to avoid the complexity of sensor-less control.

The ACE-128 absolute contact encoder by BOURNS was chosen for initial tests due to its low cost and high accuracy. The ACE-128 is a 10 pin device, two of which are the "common" pins, the other 8 pins are either an "open" or "closed" switch. When the switch is open representing a 1, the resistance between the pin and the common is at a minimum of 100 kΩ and when the switch is closed the resistance between the pin and common is a maximum of 5Ω. Therefore, by placing 1 kΩ pull up resistors between each pin and 3.3 V, the output voltage from each pin will be greater than 3.27 V and less than 0.016 V. These voltage levels are well within the ranges required for the MCU's GPIO pins to register a 1 or 0 state. Additionally, the maximum contact current and power ratings of 10 mA and 0.1 W had to be considered. A maximum contact current of 3.3 mA was calculated using the 1 kΩ pull-up resistor with a 3.3 V drop over it, where the 5 Ω resistance is neglected as it is a maximum. To calculate the maximum power, the 5 Ω resistance is now multiplied with the square of the maximum contact current, resulting in a maximum power of 54.45 μW. From the values attained for maximum current and power it is clear that a 1 kΩ pull-up resistor falls within all the required parameters. The described circuit can be seen in Figure 5.25a, with the PCB seen in Figure 5.25b.



(a) ACE-128 Circuit.

(b) ACE-128 PCB.

Figure 5.25: ACE-128 circuit and PCB.

To connect the new angle sensor to the rotor shaft an adapter was made which is simply glued to the rotor shaft. This adapter can be seen in Figure 5.26.

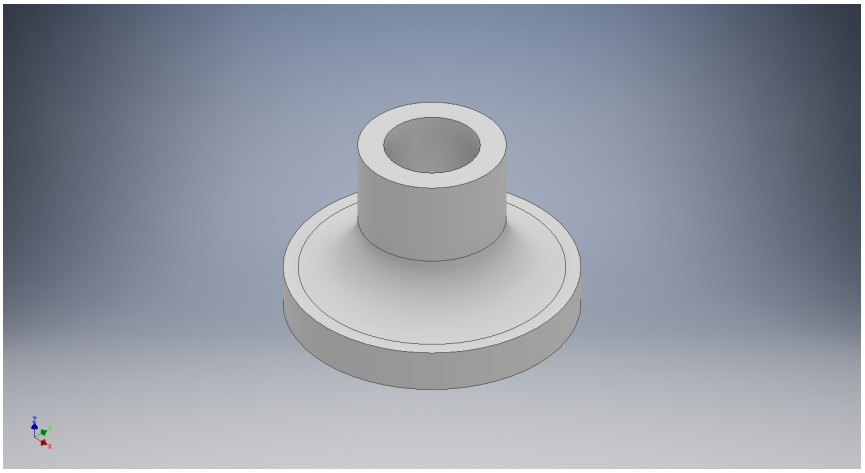


Figure 5.26: Rotary encoder to rotor shaft adapter.

The entire 3D printed assembly, as well as the PCB, can be seen mounted to the PMSM in Figure 5.27 below.

Figure 5.27: Rotary encoder assembly mounted to PMSM.

5.7 Challenges and recommendations

5.7.1 Section overview

There were a number of challenges that were encountered during the testing of the PMSM drive. Solutions were devised and implemented in the design of a second revision. However, there was insufficient time to manufacture a second revision and attempts were therfore made to fix these issues with the current design.

5.7.2 Electromagnetic interference

Electromagnetic fields are created within every electronic component due to the change of currents through conductors. However, in high current switching devices, this can cause anomalies within the device. These anomalies are due to the currents induced in nearby conductors which in turn, due to their resistance, causes a voltage to occur. The best course of action to resolve this is to reduce the EMI generated within the device, thus reducing the effects it has on surrounding circuits. Although this will eliminate any issues during controlled testing, EMI protection is still required due to unforeseen external EMI sources.

The induced voltages can in some cases be high enough to seriously alter the digital value of a signal. This was experienced on the traces between the MCU and the low side MOSFET drivers. The induced voltage resulted in the enabling of both the high side and low side drivers simultaneously. As a consequence a short circuit between the positive and negative supply rails was created. The reason such a high voltage could occur is due to the length of the traces exposing them to a greater amount of EMI as well as increasing their resistance. To solve this the ground plane surrounding the traces was improved resulting in a high level of shielding from EMI.

In the process of improving the ground plane, it was identified that two separate isolated grounds made this very complex and ineffective. Therefore, after considering the complexities of having two isolated grounds, versus isolating the external inputs. It is recommended for the revised design to isolate the external inputs to the PMSM drive. Additionally, this could reduce the total cost of the PMSM drive as the expensive isolated operational amplifiers will no longer be needed. It is further recommended to change the upper PCB to a four-layer PCB, and the lower PCB to a two-layer PCB, each of which with a dedicated ground layer. This will allow for a lower resistance to ground for all components as well as ensuring there are no ground loops.

Although attempts were made to improve the ground plane across the entire design, a number of analog circuits were still affected by EMI. Most active analog components such as operational amplifiers have high impedance inputs. As a result of this, circuits using them are very susceptible to EMI. Therefore, resistors were added between analog nodes and ground to reduce their impedance. Careful consideration was taken to make sure not to alter the operation of the circuit. As previously discussed it is recommended to keep traces between analog components as short as possible. However, this poses a significant challenge due to the MCU being some distance from a number of analog components. Therefore, an investigation into using dedicated analog-to-digital converters should be done. This is recommended as a dedicated ADC can be placed close to the analog circuitry and accessed by the MCU using less EMI susceptible digital methods. Another method of eliminating the effects of EMI on analog circuitry is to use a differential signal which uses two separate traces in which to transmit the analog value. To attain a value they are subtracted from one another thus, as long as the traces are kept close to each other noise will be identical on both signals.

In rare cases where there are very high amounts of electromagnetic radiation, such as nearby lightning strikes or direct static shocks. The circuits within the PMSM drive may be exposed to voltages well above their maximum ratings. For this reason, it is recommended for the revised design to place transient voltage suppressors (TVS) on all sensitive components as well as supply rails. An added benefit of placing TVS diodes on the supply rails is the protection to overvoltages should a voltage regulator malfunction. However, TVS diodes will sink large amounts of current to maintain the voltage they are rated for and thus, a resettable thermal fuse should be placed at the output of each voltage regulator. Although this can cause the VSD to not function for periods of time if there is a fault, methods such as these can reduce costs of device repair due to warranty.

5.8 Chapter summary

This chapter covers the design of the upper and lower PCB's of the VSD. Each of these PCB's is discussed in detail with important sections such as MOSFET drivers, current sensing and ground isolation focused on. Additionally, the cross compatibility between the designed VSD and the current VSD used by Mellowcabs is discussed briefly, as it is a key factor in many of the form factor decisions made. Some additional hardware was designed such as an external rotary angle sensor. This was done to remove the need for sensor-less control, thus aiding in the speed of development and testing.

The hardware designed in this section presented a number of faults, primarily due to insufficient ground connections between ground planes. This resulted in the effects of EMI to be severe causing malfunctions. To solve this, solder jumps were made in many places to connect ground planes. Following these modifications the only problem still experienced by the VSD was noise on the current sensors. This noise was directly correlated to the switch node voltage ringing of each phase. By reducing the switching times the voltage ringing was eliminated as well as the noise on the current sensors.

Chapter 6

Firmware

6.1 Introduction

This chapter covers the firmware written for the TMS320F28053 MCU from Texas instruments. In section 6.2 the system overview is be discussed. After which the system initialization and interrupt routine are be focused on in sections 6.3 and 6.4 respectively. Finally, each fundamental system component is further discussed from a firmware perspective in section 6.5.

6.2 System overview

Figure 6.1 below shows the flow of the entire system. From this, it can be seen that the firmware is broken up into two primary sections. The first section is the startup process, where all peripherals are initialised, required delays implemented and the calibration process is completed. The second section is the interrupt service routine. This can be seen as an infinite loop where all of the sensor readings and motor control takes place.

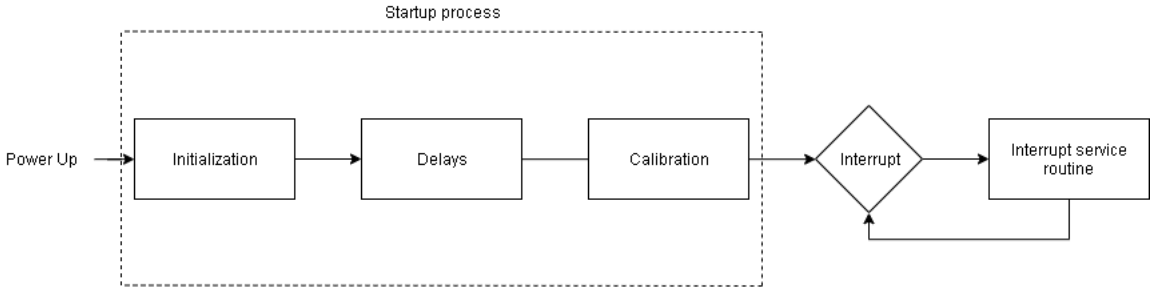


Figure 6.1: System overview flow diagram.

6.3 System startup

The system clocks are the first component to be configured during the initialization process. The prescaler for the internal oscillator is configured to one, resulting in a system clock of 10 MHz. Following this, the phase lock loop is enabled multiplying the system clock to 60 MHz. After the clocks have been configured, the general input-output pins are configured to their required states. During this process, the internal pull-up or pull-down resistors are enabled if required. The next step in the initialization process is to configure the analog to digital converter module, this is covered in more detail in section 6.5.3. Lastly, the six

enhanced pulse width modulation modules are configured to output a synchronised signal with a configurable frequency between 10 kHz and 50 kHz. This is focused on in more detail in section 6.5.4.

After the system initialisation has taken place, a short delay is implemented. This is done to allow the system to normalise, ensuring accurate calibration. The calibration process involves the measurement of signals from components such as the voltage and current sensors from each phase. This is required as their outputs have an offset of half their supply voltage, which typically has a 5% tolerance. This offset is then used for all subsequent measurements to determine the true value.

The short delay mentioned above was later extended to two seconds for development purposes. This allows for the possible firmware update process to begin before the interrupt service routine executes for the first time. This has to be done in case there is an issue with the firmware resulting in an over-current condition. An over-current condition will cause the power supply to current limit, resulting in an MCU brown out reset. Without the two-second delay, it is impossible to start the firmware upload process between MCU brown-out resets. Thus, it would not be possible to update the firmware making the firmware issue permanent.

6.4 ePWM interrupt service routine

The operational flow of the ISR can be seen in Figure 6.2. Although the ISR does not contain any physical loops it is indicated as an infinite loop. This is to aid in the explanation of the ISR as it is called from the ePWM module after three ePWM periods have occurred. Thus, the ISR is called repetitively between 3333 and 16666 times a second depending on the switching frequency.

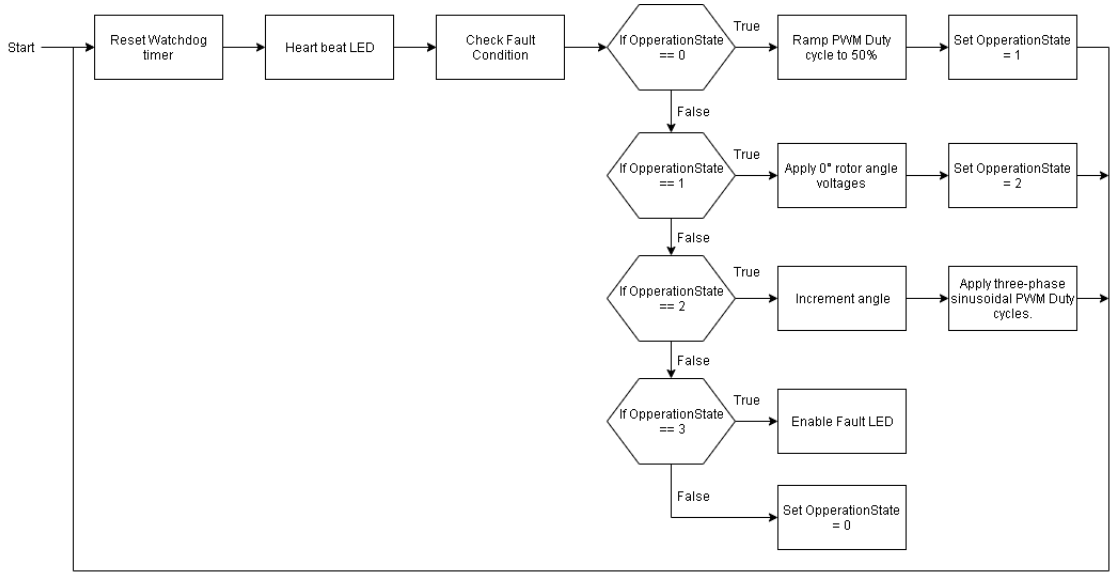


Figure 6.2: ISR flow diagram.

The first task which is executed within the ISR is to reset the device watchdog. The watchdog is a hardware counter which is incremented by the system clock. Once the counter reaches a set value, a forced MCU reset is executed. Therefore, for a reset to not take place the watchdog timer must be cleared regularly. If a bug within the firmware such as an infinite

loop occurs, the watchdog timer is not cleared and the MCU will reset. This adds a layer of reliability and error handling to the firmware.

Directly after resetting the watchdog timer, a counter for the heartbeat LED is incremented. A counter is needed, because if the LED were to be toggled on each ISR execution, the change of state would not be visible. Thus, the counter acts as a prescaler for the LED's toggle frequency.

The next stage of the ISR algorithm is to check for a fault within the three-phase inverter. This is achieved by subtracting current sensors 1 and 2 of each phase from each other. If the value falls outside the range of $-30\text{ A} < I_1 - I_2 < 30\text{ A}$, there is then a significant current imbalance within the system. If a fault condition occurs, the operational state variable of the drive is set to three and the ePWM modules are disabled. It is recommended to develop this feature further to identify potential issue and place the drive in a limp-home mode if possible. This reduces the risk of a stranded vehicle should a drive malfunction take place in the Mellowcabs application.

The final stage of the ISR is the switch case in which the task executed depends on the current state of the drive. The state of the drive is determined by the integer value stored in the variable OpperationState as seen in Figure 6.2. The operation performed during the first state is to simultaneously ramp the ePWM duty cycle of each phase to 50%. During this state, the fault detection stage monitors the phase current to ensure they are all within $-10\text{ A} < I < 10\text{ A}$. This can be done, because the ePWM duty cycles of each phase increase simultaneously, thus there should be minimal phase currents unless there is a hardware fault.

The second operational state performs the task of calibrating the rotor position sensor. This is done to ensure correct operation should the sensor not be properly aligned during the assembly of the machine. The calibration process involves applying the voltages of 0° to phase A, 120° to phase B and 240° to phase C, at a low modulation index. Thus, locking the machine at one of the three mechanical rotor angles resulting in an electrical angle of 0°. This state is held for a minimum of half a second and until the rotor angle becomes constant. However, if the rotor angle is not constant within two seconds of entering the state the previously attained calibration value is used. The modulation index for this state is chosen to allow a current of approximately 30 A peak to peak per phase. Additionally, the parameters for the fault detection phase are set to $-10\text{ A} < I_1 - I_2 < 10\text{ A}$. This also allows the detection of hardware issues before the drive is placed into a fully operational state.

The third state is the full operation of the drive, this is the state in which FOC is implemented. However, for the testing done in this thesis to verify the results found in chapter 4 FOC was not implemented. Instead a simple three-phase sinusoidal signal with a limited modulation index was implemented.

6.5 System components

6.5.1 Section overview

In this section the firmware required for the operation of each of the fundamental components is discussed. These fundamental components are the rotor sensor, analog to digital converter and the enhanced pulse width modulation.

6.5.2 Rotor angle sensor

With the eight available outputs from the ACE-128, the angle of the shaft can be represented as a number between 0 and 255. However, the ACE-128 only has 128 angle positions, therefore a mechanical resolution of 2.8125° and an electrical angle resolution of 8.4375°is attainable. This results in a much higher accuracy than available from the hall effect sensors, thus making the implementation of FOC much simpler.

As a result of the mathematical operations that take place within the ACE-128 the output data does not directly correlate to the angle value between 0 and 127. For example, the output value of 1 is angle position 56 and the output of 2 is angle position 40. To solve this a simple method of using a 256-byte lookup table was implemented. Within this truth table the angle value is stored in the table at the address that corresponds with the ACE-128 output value.

6.5.3 Analog to digital converter

The analog to digital converter module used in the TMS320F28035 is a 12-bit recyclic ADC. This ADC operates using part successive-approximation-registers and part pipelining. The core of the ADC module is made up of a single 12-bit converter which is fed by two sample and hold circuits. Each of the sample and hold circuits can be utilised simultaneously or sequentially. Thus, due to the configuration of the ADC core, a maximum of two ADC samples can be taken simultaneously. The sample and hold circuits are fed with up to 16 analog inputs thus requiring up to eight sample sequences to take place to read all inputs. This is however simple to do on the TMS320F28035 as a series of conversions can be triggered from a single event. Each of these conversions is individually configured with the configuration known as a Start-Of-Conversions (SOC).

The SOC's can be configured to be triggered by several sources such as GPIO's, CPU timers or ePWM events. Due to the nature of a PMSM drive, it was chosen to trigger the ADC sampling with the ePWM. This allows for synchronous sampling with the PWM output as well as reducing the complexity of having to configure additional CPU timers.

Each SOC can be configured to have a different sample and hold window size. This is to allow circuits with a high output impedance to properly charge the sample and hold circuit. The compromise to this is an increase in the total ADC sample time. The lowest sample window size of 6 was chosen for this application allowing the fastest possible sample rate. This can be done due to the analog hardware being sampled having a relatively low output impedance.

The total time taken to sample an ADC input is comprised of the sample window time and the conversion time. With a clock frequency (f_{clock}) of 60 MHz and a window size (W_{size}) of 6, the total sample window time (T_{SW}) is

$$T_{SW} = (W_{size} + 1) \times \frac{1}{f_{clock}} = 7 \times \frac{1}{60 \times 10^6} = 116.667 \text{ ns}. \tag{6.1}$$

The ADC conversion requires a total of 13 clock cycles thus, the conversion time is 216.66 ns. Therefore, the total time to get an ADC value is 333.33 ns. However, the value of two sample and hold windows can be acquired simultaneously. Thus, the total time to process two ADC values is $116.667 + 216.667 \times 2 = 550$ ns, averaging it to 275 ns per ADC value. Knowing this with a total of 12 ADC inputs to sample, the total acquisition time of all the ADC inputs is 3.3 μs.

The ADC can operate with either an external or internal reference voltage, where the input reference voltage operates between 0 V and 3.3 V. It is important to note that the VREFLO pin must be tied to ground in this mode. In the 56 and 64 pin TMS320F28035 this can be done internally, however, on the 80 pin device such as used in this application the pin must be tied low externally.

ADC calibration

Any ADC converter will inherently have a zero offset error as well as a gain error. This is compensated for by Texas Instruments by performing a calibration at 30° C during manufacturing at the factory. However, although the ADC converter may be calibrated, a calibration process still has to be performed due to tolerances in components such as resistors and voltage regulators. Thus, the following method of calibration was developed.

It was decided to first perform the calibration on the input voltage reading as for simplicity of testing this had to be done before the large input capacitance was added. To begin the calibration process data was needed to investigate the output error and how to compensate for it. An input voltage ranging from 11 V to 59 V was applied to the inverter at approximately 1 V increments. At each increment, an accurate reading of the input voltage was taken as well as the ADC result.

By analysing this data it could be seen that the ADC result did in fact have a DC offset with a linear gain error. Thus to correct this error two samples are used to formulate an equation as follows,

$$y = (x - a_1) \cdot \frac{v_2 - v_1}{a_2 - a_1} + v_1 \tag{6.2}$$

where y is the calibrated ADC value, x is the raw ADC result, v_1 and v_2 represent measured voltages of the two samples and a_1 and a_2 represent the raw sampled ADC values.

ADC conversion calculation

The sampling and conversion of the ADC values, as well as an ISR are triggered by the ePWM. Within this ISR the ADC values are read from their respective registers and are converted to relevant voltages or currents.

Due to the ADC having a 12-bit resolution the 3.3 V input value will be represented by a value between 0 and 4095. Knowing this, all inputs had to be multiplied by the resolution of 3.3/4095 as well as any scaling factor and offset due to hardware such as resistor dividers or isolated amplifiers. Once the values have been calculated they are stored in globally accessible variables, allowing the control algorithms to access the latest value at any time.

6.5.4 Enhanced pulse width modulation

The TMS320F28035 ePWM peripheral is comprised of multiple individual ePWM modules. This allows for each ePWM module to be highly programmable while reducing the CPU overhead. This however, adds complexity to the initialisation process as each individual module needs to be configured separately. Additionally, as the ePWM modules are individual it is possible for them to be out of sync. Thus, a method using a synchronising signal is used between each module. The synchronising signal functions as seen in Figure 6.3, where it can be seen that the signal passes through each module onto the next. Due to this, it is required that the signal must be able to pass through the ePWM module regardless of if it synchronises with it. This allows module three to sync with module one while module two

is independent. To enable the synchronisation of the module with the signal the PHSEN bit of the TBCTL register must be set to 1.

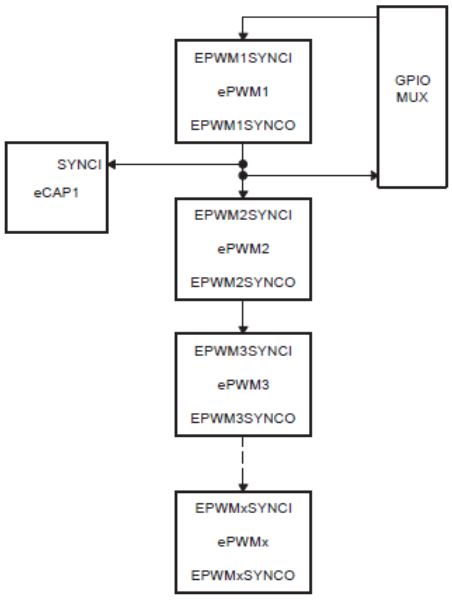


Figure 6.3: ePWM synchronisation signal path.

Within the ePWM peripheral there are two types of PWM, these being regular and high-resolution PWM (HRPWM). The HRPWM is an extension of a number of standard PWM channels which allows for up to 95 times the resolution in duty cycle. This added resolution is specifically useful in applications where very high switching frequencies are needed. However, due to the limited number of available HRPWM channels as well as the relatively low switching frequencies of the three-phase inverter, this was not used.

The PWM period is determined by a counter register counting up on each clock cycle. This is done until the value of the counter reaches the value set in the TBPRD register. Following this, the counter is then set back to zero and the process begins again. The TBPRD register is an unsigned 16-bit integer, thus having a maximum value of 65535. This would result in the lowest possible PWM frequency of approximately 1 kHz with a 10 MHz internal oscillator and a 60 MHz system clock. To allow lower frequencies a prescaler is available to reduce the frequency of the clock seen by the counter. It is important for the application of the PMSM drive that this prescaler is set to one due to the PWM frequency being well above 1 kHz. The duty cycle is determined by the value stored in the register CMPA. The ePWM output pin is high when the counter has a value from zero to CMPA.

The ADC and ePWM interrupts are configured to execute when the counter register of ePWM module is reset to zero. The interrupts can however, be configured to only execute the relevant ISR on up to the third occurrence of the counter being set to zero. Due to the total time required to sample all the ADC inputs being 3.3 μs, which is significantly less than the switching period of 50 μs, the ADC ISR is triggered every zero reset. However, the ePWM ISR is configured to only execute every third zero reset occurrence. This is due to the time taken for the moderately complex FOC calculations to take place.

The final aspect of the ePWM module which was configured is the Deadband. As a result of the C2000 family of micro-controllers being aimed at switching applications. The ePWM modules have configurable Deadband built into the ePWM hardware module. The Deadband

can be configured to have unique rising and falling times, which can aid in reducing body diode conduction losses if different deadtimes are used.

6.6 Chapter summary

This chapter covers the firmware design and implementation for the VSD. The chapter begins with a flow diagram giving a brief overview of the system software which can be seen in Figure 6.1. The chapter then covers the startup and interrupt service routine in detail as these are the two primary sections of software. Following this the chapter focuses on the software for the peripheral components required for the VSD.

Chapter 7

Simulated vs actual thermal results and thermal resistance

7.1 Introduction

The focus of this chapter is placed on final thermal simulation and testing. It begins with a test and simulation to asses the validity of the thermal simulations. Following this, a thermal simulation is performed to find the thermal resistance of the VSD. Finally a thermal simulation is performed to show an example of how the end user can benefit from a thermal model of the VSD.

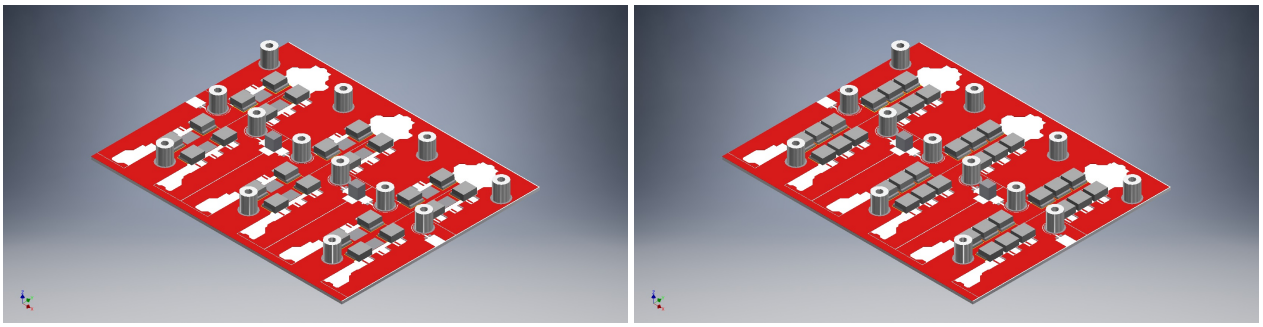
7.2 Thermal simulation verification

7.2.1 Section overview

To asses the validity of the thermal simulations of the VSD a controlled test was performed. In this section the test as well as the results are discussed. The test involved operating the drive in a highly inefficient manor to create high losses similar to what would be seen under normal operation conditions, without the need for a load. During the test the losses as well as temperature were measured. These losses were then entered into a CFD simulation to determine the corresponding simulated temperature. With this information it was then possible to make a comparison between the simulated temperature and the actual temperature.

7.2.2 Simulated vs actual thermal results

The PCB design chosen for the VSD can accommodate six parallel MOSFETs per inverter switch. Although this is not needed as the optimal design only requires four MOSFETs placed in parallel. This allows for the testing of higher power applications and alternate MOSFET configuration options. Due to the similarities between the four and six MOSFET designs, this can be achieved by not populating some of the MOSFETs, as seen in Figure 7.1 bellow.



(a) 24 MOSFET design. (b) 36 MOSFET design.

Figure 7.1: Final design of PMSM drive.

A low frequency three-phase sinusoidal signal was applied to the motor. This allowed for a controlled speed as well as high losses at low power due to the inefficiency of this method of motor control. It is key to note that the total power at which the drive is operated at is irrelevant to this test, as heat is directly related to losses. Due to the design process focusing on the thermal resistance of the VSD, allowing the end user to choose a cooling solution that fits their application. The test is done without a heatsink to focus on only the VSD. As a consequence of this, the test must be performed at between 30% and 40% of the full power losses to prevent over heating.

In order to determine the total losses in the VSD, the power entering the PMSM was subtracted from the total power supplied to the drive. To measure the total power supplied to the PMSM, the two-meter method was used. This involves measuring I_a, I_c, V_{ab} and V_{cb} as seen in Figure 7.2.

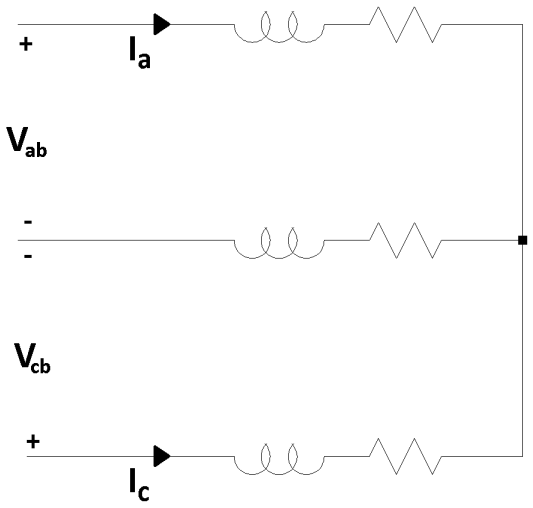


Figure 7.2: PMSM measurements.

With these values, the real power being used by the PMSM can be calculated as

$$P_{output} = P_1 + P_2 \tag{7.1}$$

where,

$$P_1 = \frac{1}{N}\sum_{n=0}^{N} V_{ab}(n) \cdot I_a(n) \tag{7.2}$$

and

$$P_2 = \frac{1}{N}\sum_{n=0}^{N} V_{cb}(n) \cdot I_c(n). \tag{7.3}$$

A summation is used to determine the average powers as the measurements were taken using an oscilloscope and saved to a CSV file. This data was then imported into a Matlab script to solve for P_{output}. The same method was used to measure the power supply voltage and current, after which P_{input} is calculated in a script as

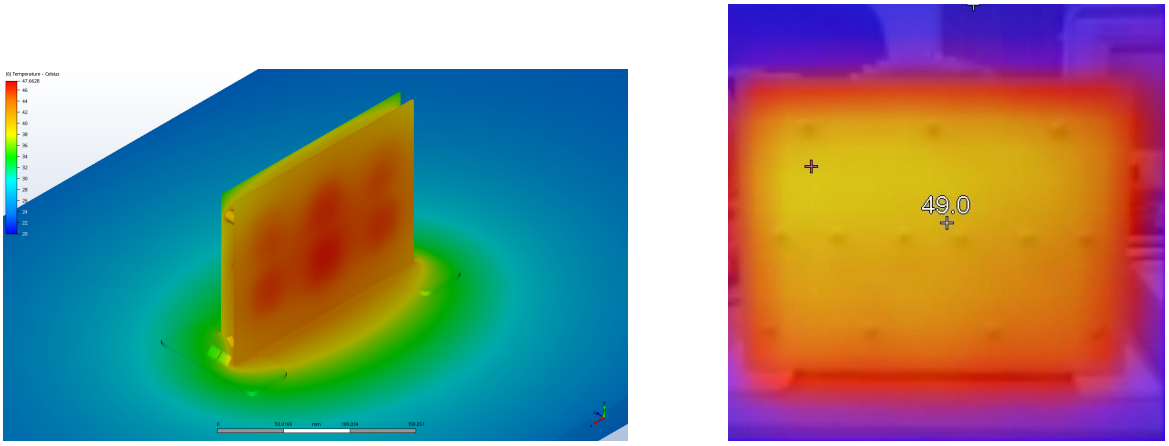
$$P_{input} = \frac{1}{N}\sum_{n=0}^{N} V_{supply}(n) \cdot I_{supply}(n). \tag{7.4}$$

Thus, the losses can be calculated as

$$P_{losses} = P_{input} - P_{output} = 61.61 - 15.07 = 46.54W. \tag{7.5}$$

With the total power losses attained, the thermal simulation was run. It was important to place the upper PCB and table in the simulation as they reduce the effects of heat transfer through the air. The air volume was created with a size of 3 m^3, and the boundaries set to the actual ambient temperature of 20.1 °C.

A thermal camera was used to get an equivalent image of the actual PCB once it had reached temperature equilibrium. A comparison of the simulation and actual measurements can be seen in Figure 7.3.



(a) Results from thermal simulation (Max temp: 47.66 ° C).

(b) Results from the three-phase inverter test (Max Temp: 49.8 °C).

Figure 7.3: Thermal simulation vs actual results.

The hot spots seen in the simulation cannot be seen in the image from the thermal camera. This is due to the temperature range being too large and thus the hot spots are unidentifiable. However, from this test it can still be concluded that the actual temperature reached by the

VSD is approximately 2.14 °C warmer than the simulated test. This result is considered to be within acceptable range to validate the thermal simulations. There are a number of factors which could be further investigated to potentially reduce this error. The first of which is the accuracy of the thermal camera's calibration. Secondly, tests should be done to further investigate factors such as the thermal resistance of the solder used in placing the MOSFETs on the PCB.

7.3 Thermal resistance simulation

To determine the thermal resistance of the drive ($R_{\theta Drive}$), a similar method will be used as in Section 4.4. An infinite heat sink will again be simulated by using a 500 mm x 500 mm x 3 mm aluminium plate with a surface temperature fixed at 25 °C.

From Figure 7.4 a maximum temperature of 36.139 °C was seen. From this as well as knowing the total losses in the VSD, the thermal resistance can be calculated by

$$R_{\theta Drive} = \frac{Max\ Temp - Ambient}{Total\ Losses} = \frac{36.139 - 25}{211.5} = 0.052667\ ^{\circ}\text{C/W}. \tag{7.6}$$

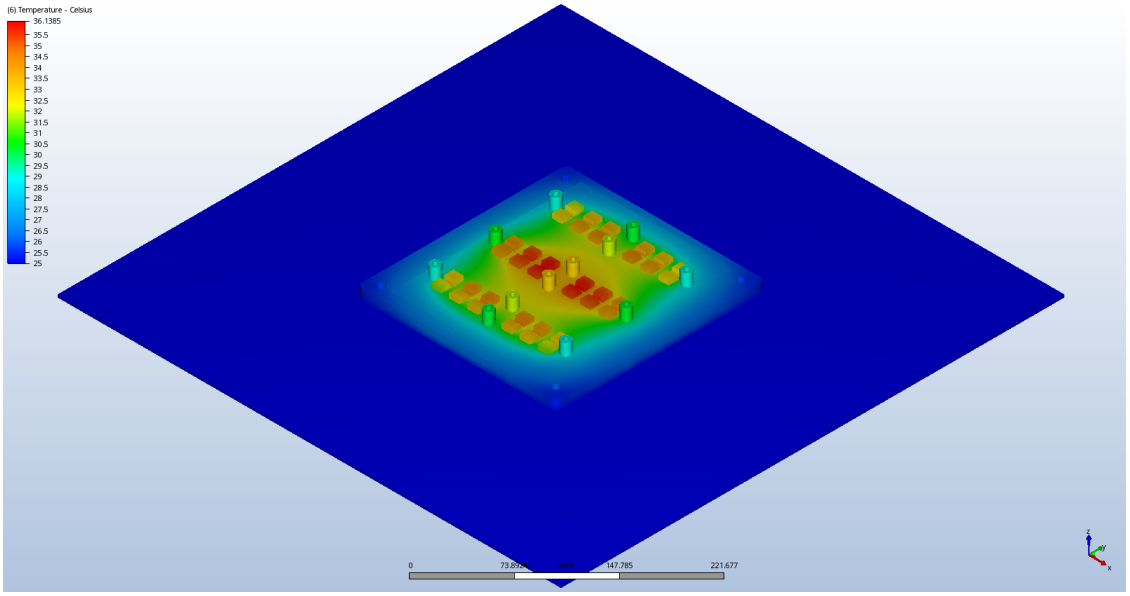


Figure 7.4: Motor drive temperature with infinite heatsink.

Using this thermal resistance value, the end user can design a cooling system specific to their application. This is key for applications such as high temperature environments or tight spaces.

7.4 Example of thermal simulations in VSD applications

An investigation was done into the need for a heatsink in the Mellowcabs application. To do this the rear member of the Mellowcabs chassis was modeled in Autodesk Inventor. Again the thermal interface materials used in Section 4.5 were added between the VSD and the rear chassis member. Due to the size of the rear chassis member, the size of the air volume had to be increased to 3 m^3. Figure 7.5 shows the results of the simulation where it can be seen that a temperature of 89.41 °C was reached with an aluminium thickness of 3 mm.

This is substantially lower than 175 °C and in fact lower than the temperature reached with the heatsink as seen in Table 4.3. It is also important to note that there are multiple other aluminium plates mounted to this chassis member which will aid in the dissipation of heat.

An additional benefit of the removal of the heatsink is a reduction in maintenance. This is due to road dirt greatly reducing the effectiveness of heatsink fins, thus the heatsink regularly needs to be cleaned. Further investigation should be done into the effects of convection cooling when the vehicle is in motion, due to the high airflow speeds from the rear diffuser effect at this panel.

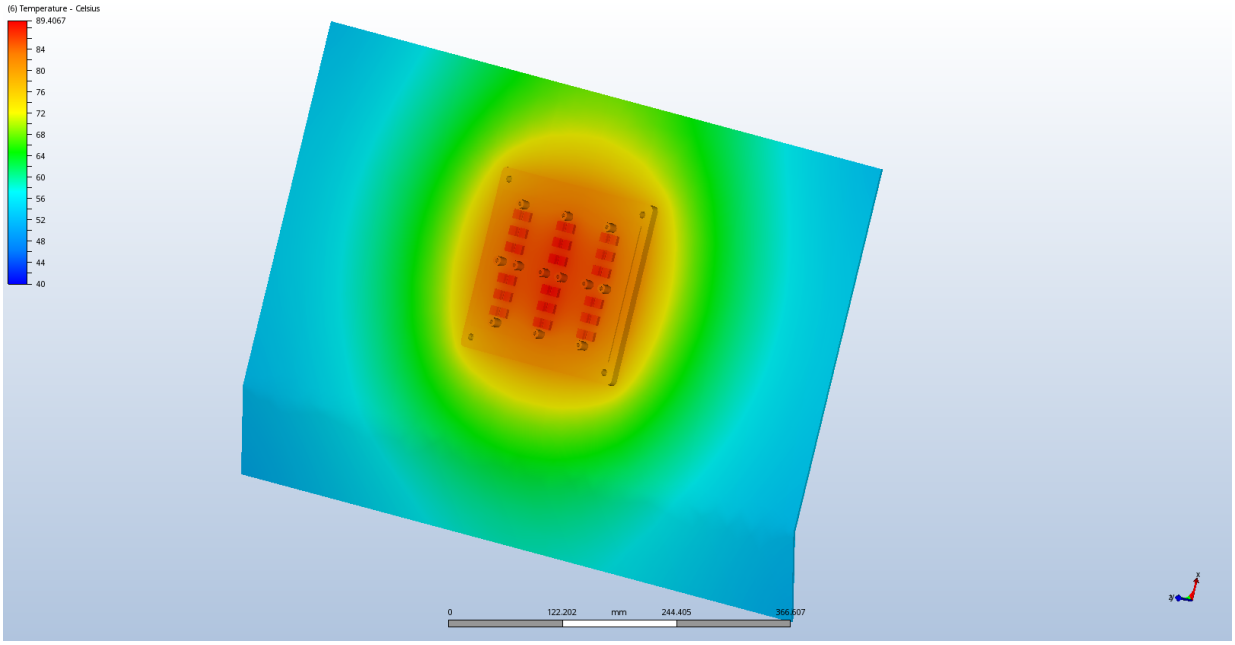


Figure 7.5: Motor drive temperature with Mellowcabs rear chassis member.

7.5 Chapter summary

In conclusion, it can be seen from the test performed that the thermal simulations are sufficiently accurate. However, further investigation can be done to improve this accuracy. The thermal resistance is successfully attained allowing this to be added to the VSD datasheet. Using this thermal resistance or the actual thermal model of the VSD, the end user can optimise there design as shown in Section 7.4.

Chapter 8

Conclusion and recommendations

8.1 Introduction

This chapter concludes this thesis by discussing the recommendations for future work in section 8.2, followed by the final conclusion given in section 8.3.

8.2 Recommendations

8.2.1 Section overview

After the completion of the project performed for this thesis, a number of recommendations for further study in simulation were identified. These recommendations for further study are discussed in section 8.2.2. Additionally, a number of recommendations were identified for the design and implementation of the VSD. These recommended changes and modifications are discussed in sections 8.2.3 and 8.2.4.

8.2.2 Simulation

Further investigation should be done on incorporating the calculations for switching losses within the Simulink simulations. This will greatly simplify the use of the simulations, as the separate files and scripts add complexity.

It is also recommended to develop a simulation to investigate the switch node ringing, allowing the reduction of this before the design is built. This should also be incorporated into the simulations for losses as it was neglected in this thesis.

8.2.3 Hardware design

During the testing of the hardware, it was identified that EMI was a large issue, in some areas completely disrupting the operation of the hardware. In section 5.7.2 this is discussed in more detail as well as the methods implemented to reduce this issue. It is thought that a large portion of this noise is as a result of the switch node ringing and thus, this is also discussed in more detail in section 5.2.5. After this, a number of hardware suggestions are made such as the addition of temperature sensors on the lower PCB as well as additional communication ports.

8.2.4 Firmware design

One of the key features identified, due to the requirement of having two current sensors per phase, is the ability to add fault detection, as well as possible limp home modes. This needs to be developed further, with the possible addition of power limiting at high unit temperatures. This allows for smaller cooling methods to be used, while still having protection if the device is placed under high loads for prolonged times.

8.3 Conclusion

During the design process of any power inverter, a compromise has to be made when choosing the switching components. These compromises are made using data available and thus, the more data available allows for a more optimal compromise to be made. Additionally, the data used during this process of switch selection is typically purely electrical, with the thermal aspect of the design being a secondary focus.

In order to make the best possible compromise in choosing a MOSFET switch for a 5 kW PMSM drive, three sets of thermal simulations were included. The first set of simulations was performed using Matlab Simulink, where the switches within the three-phase inverter were made ideal. This was done to enable the collection of data needed to set the minimum specifications for the MOSFET switches.

Once a selection of seven MOSFETs was made, the second set of simulations was performed. This set of simulations determined the total loses within the three-phase inverter for each of the seven switch options. During the process of developing the simulation, it was found that simulating the switching losses using Simulink was unrealistic. This is because an extremely small maximum iteration time has to be used. As a result, the total simulation time is unacceptably long for the use in industry. On further investigation, it was also found that the switching voltages and currents within the Simulink simulation were not correct, as seen in Figure **??**. Thus, the Simulink simulation was only used for determining the conduction losses and acquiring the data needed to calculate the switching losses. From this data the switching losses are then calculated analytically in a separate MATLAB script. Using these simulations, the total losses for each MOSFET option was successfully attained. These results are then used to identify the most efficient switch options.

After finding the losses for each MOSFET option, the focus was then placed on the thermal aspect of the design. First, a short investigation was performed using just one MOSFET to test the accuracy of the designed D2PAK thermal model. This model was then used in four different designs accommodating the varying number of MOSFETs required. These designs were optimised through the use of simulation to reduce hot spots. This is important as mentioned in section 3.2.6 temperature plays a role in the self-balancing properties of MOSFETs in parallel. Although a perfect uniform temperature between all the switches is desired. This was not entirely possible due to design restraints such as required trace widths and current sensor limitations. The PCB designs were then used to simulate each of the seven MOSFETs to compare the effects of different component counts and thermal junction to case resistances. This was done using the current cooling method used by the lightweight weight vehicle manufacturer Mellowcabs.

After the optimal switch had been chosen using the data attained thorough out the simulation process. The designed drive was then simulated to find the thermal resistance of the entire drive. This allows for a custom cooling solution to be chosen by a vehicle manufacturer should they require to do so. Additionally, the current cooling method used by Mellowcabs was

simulated along with a cheaper and lighter alternative method to determine the feasibility of this. The simulations showed that the lighter and cheaper cooling solution was, in fact, superior to the current method being used. This verifies the importance of using thermal simulations within electrical design and manufacturing.

Finally the designed hardware was tested to find the accuracy of the thermal simulations. Further investigations can be done into the slight difference in temperature between the test and the simulations. However, this temperature variance is still within an acceptable range.

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Appendices

Appendix A

Full circuit diagrams

All of the circuit diagrams for the design of the PMSM Drive can be seen in this section.

Lower PCB

The lower PCB is a single Layer PCB with an aluminium core which has mainly power components on it. The Schematic for the drivers can be seen in figure 1, current sensors can be seen in figure 2 and the MOSFET bridge is seen in figure 3.

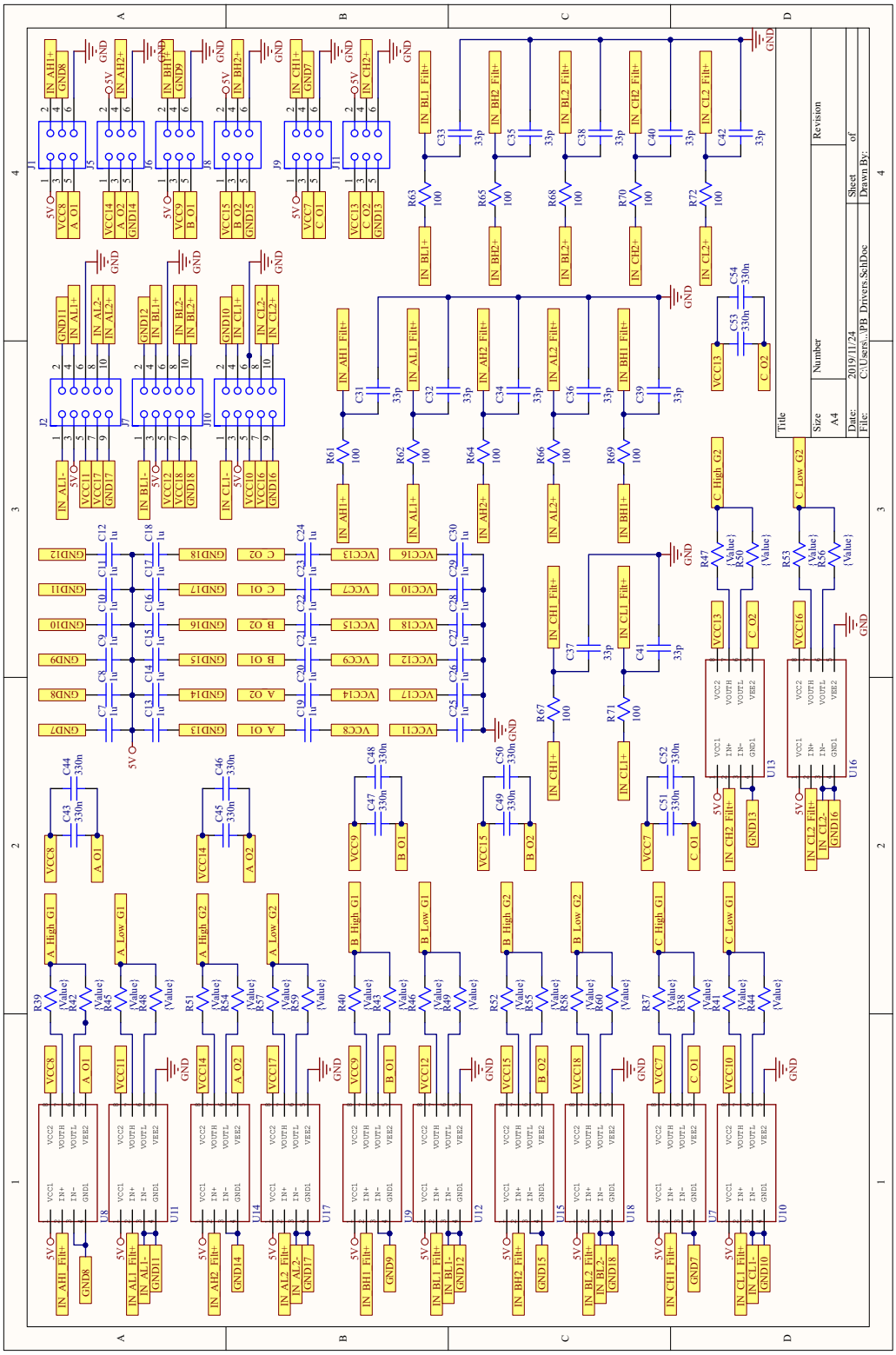

Figure 1: Schematic for MOSFET drivers

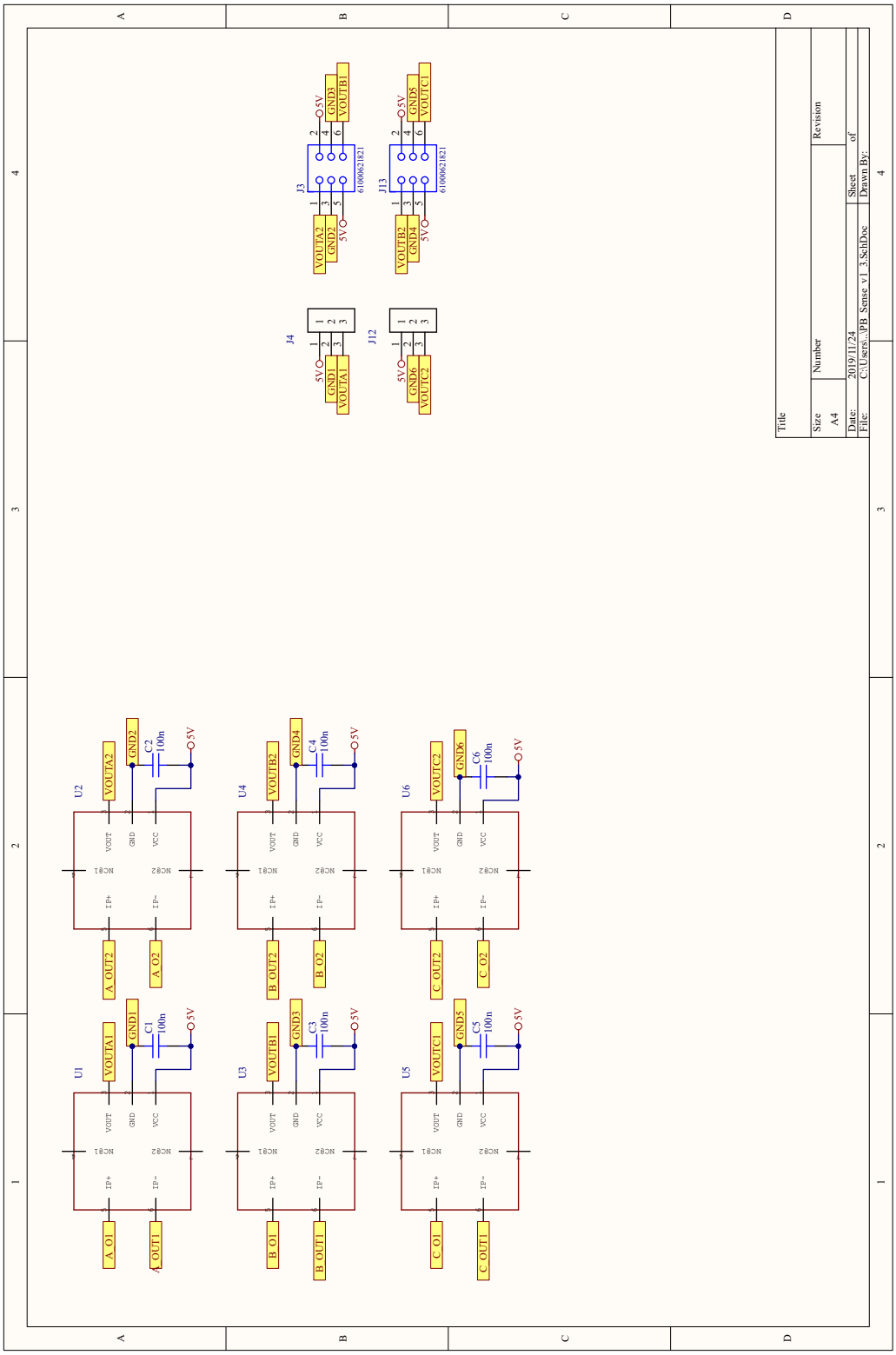

Figure 2: Schematic for current sensors

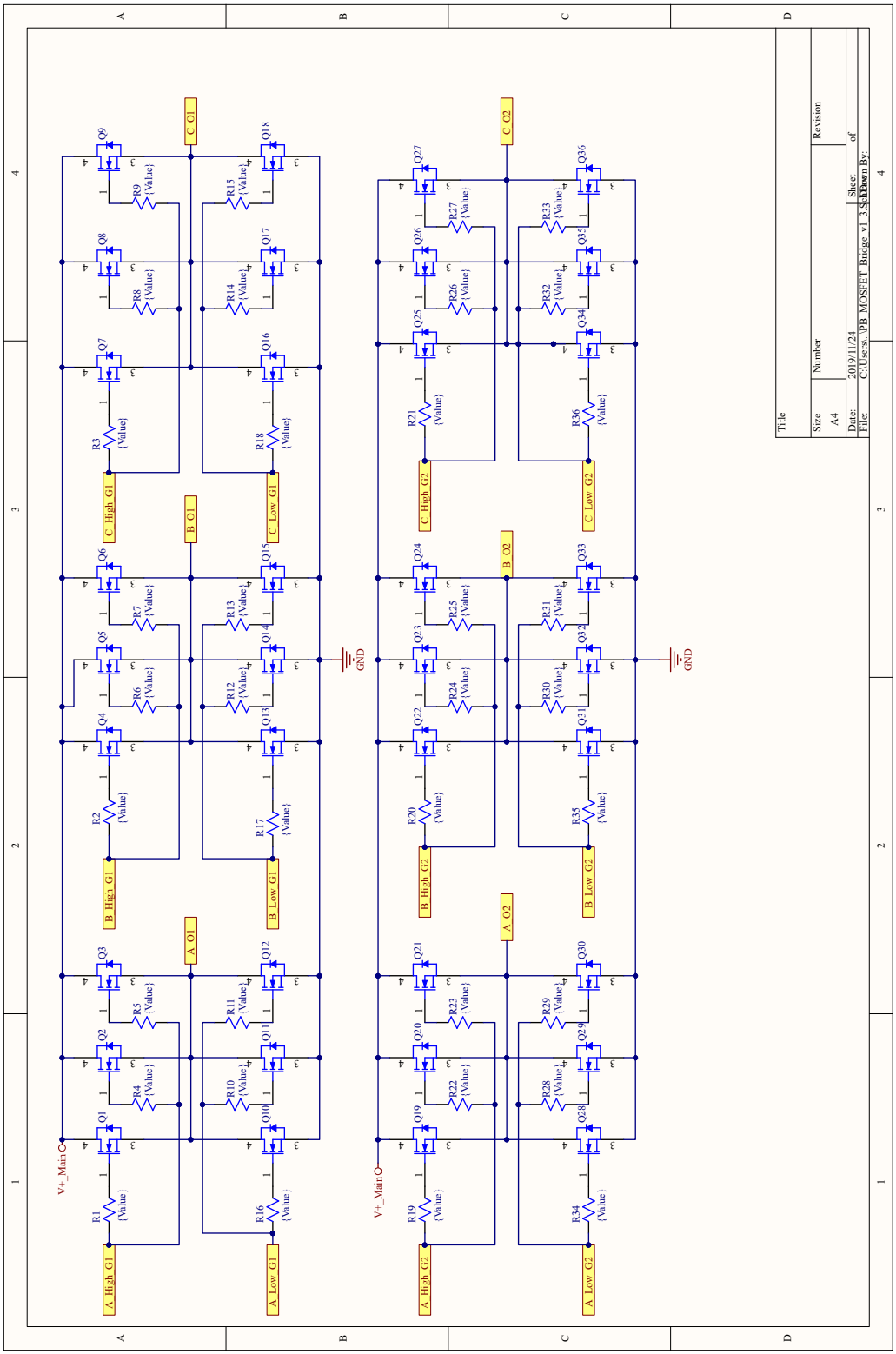

Figure 3: Schematic for MOSFET bridge

Upper PCB

The schematics for the upper PCB can be seen in figures 4 to 8.

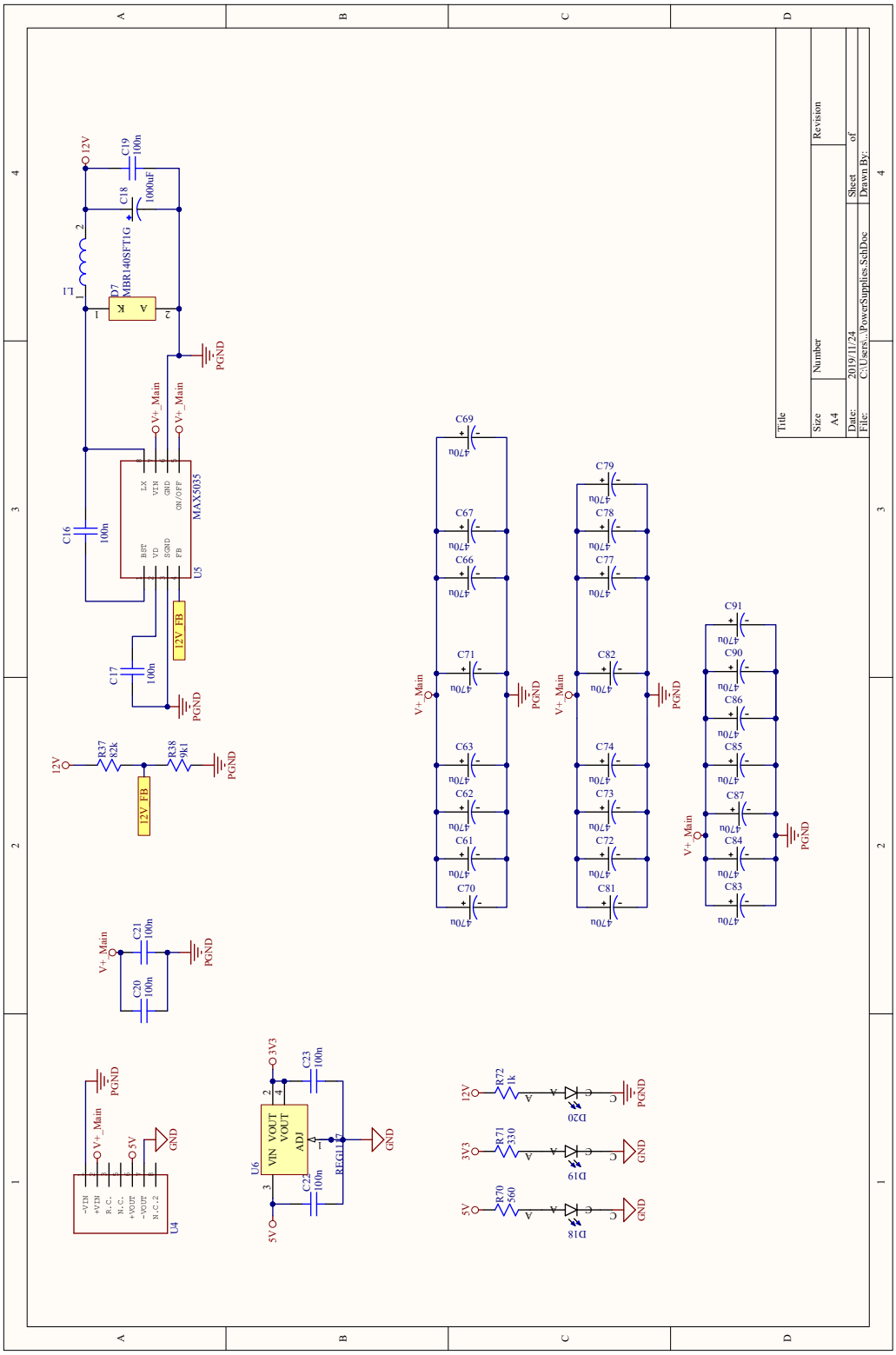

Figure 4: Schematic for voltage regulators

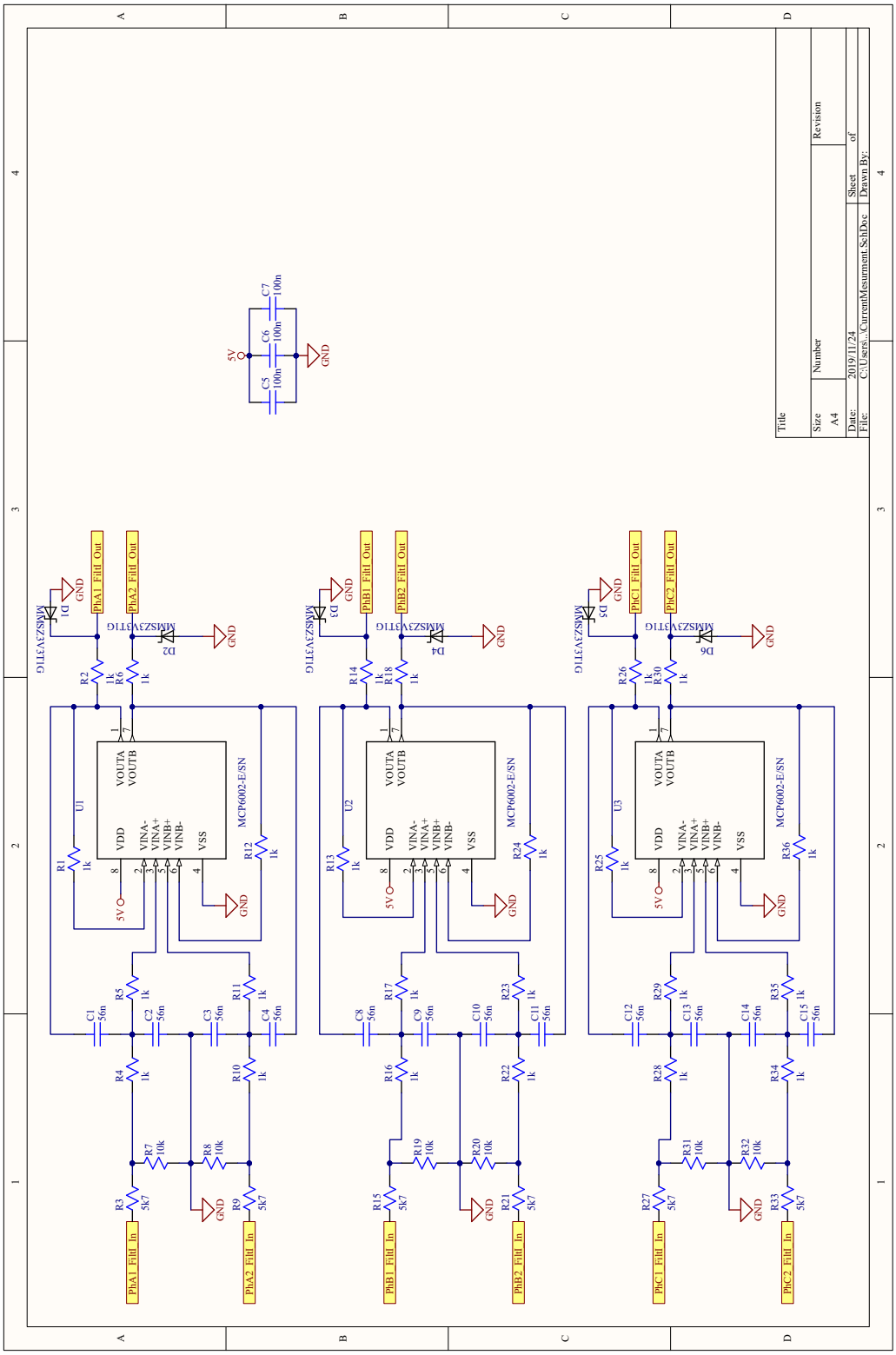

Figure 5: Schematic for current measurement

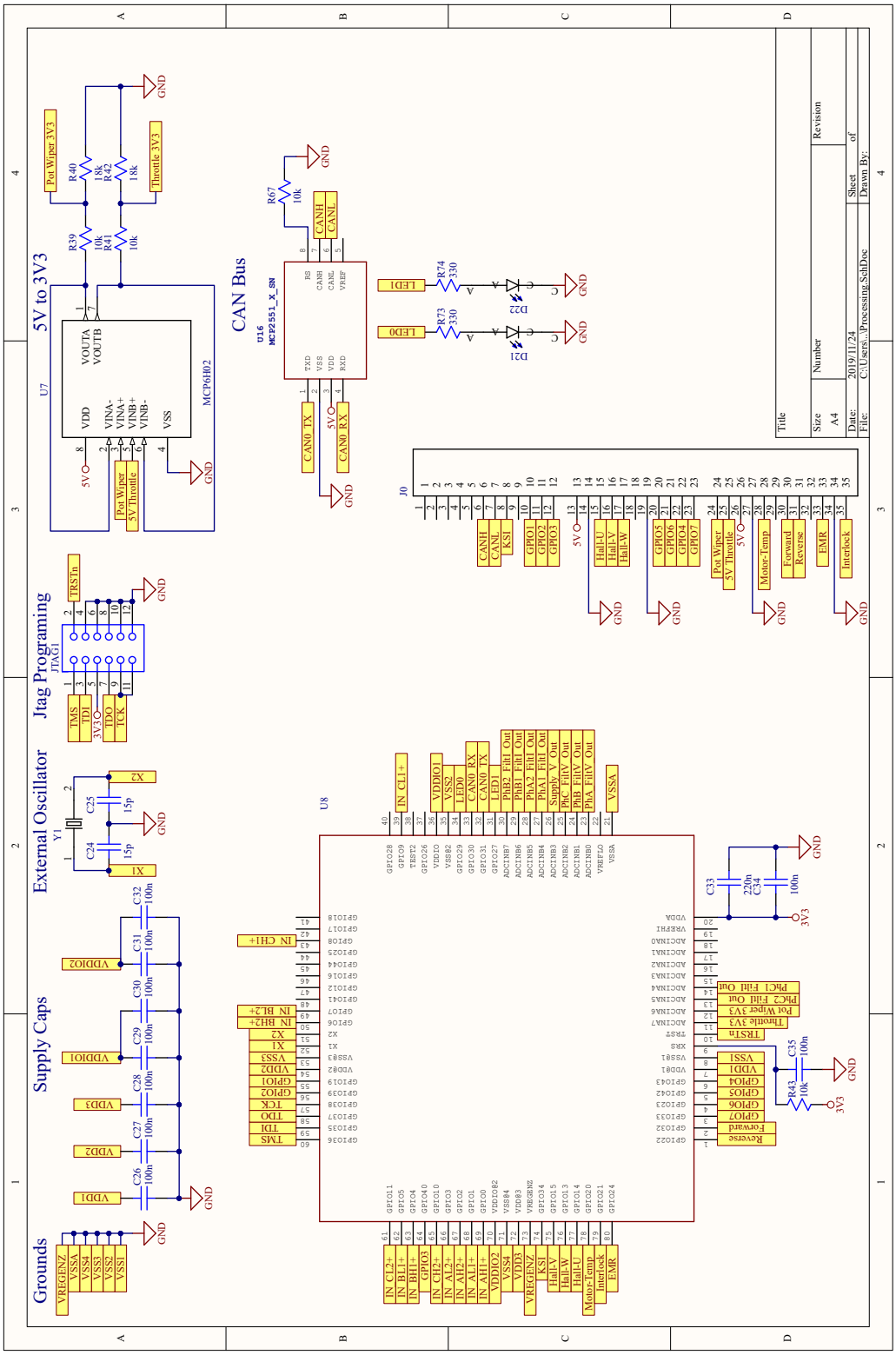

Figure 6: Schematic for MCU

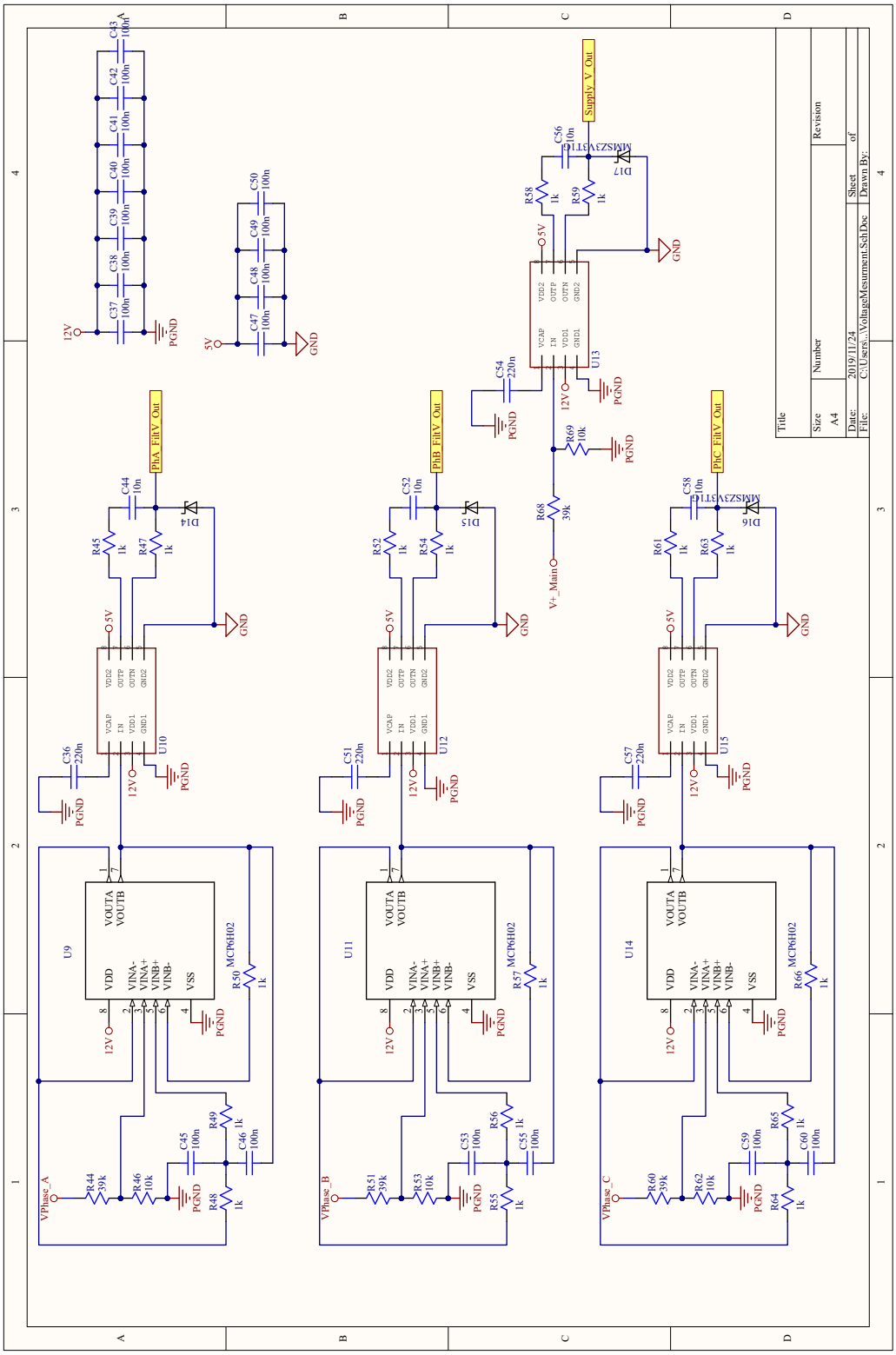

Figure 7: Schematic for voltage measurement

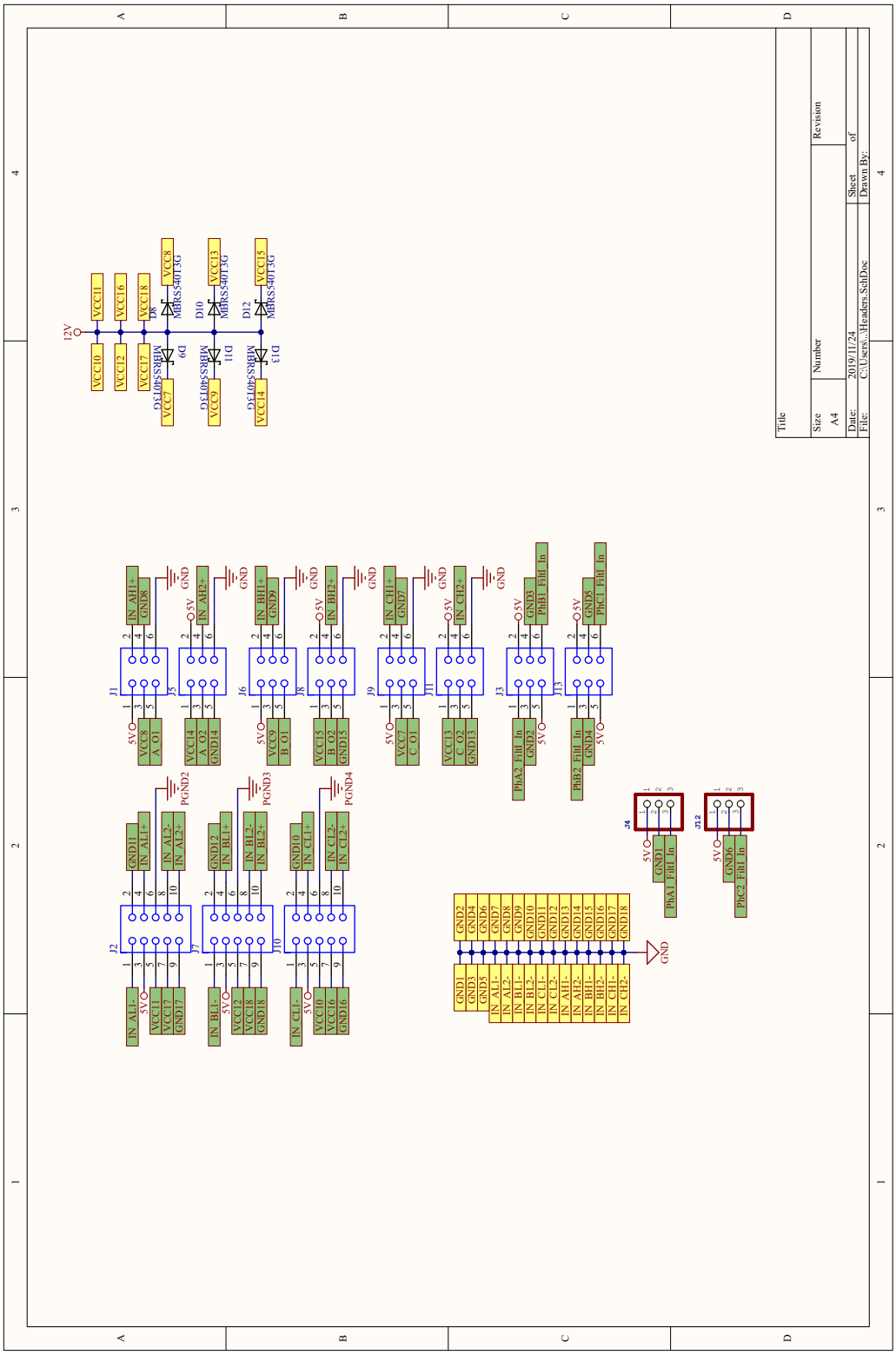

Figure 8: Schematic for headers connecting to lower PCB

Appendix B

Full PCB designs

Lower PCB

The full lower PCB can be seen in figure 9.

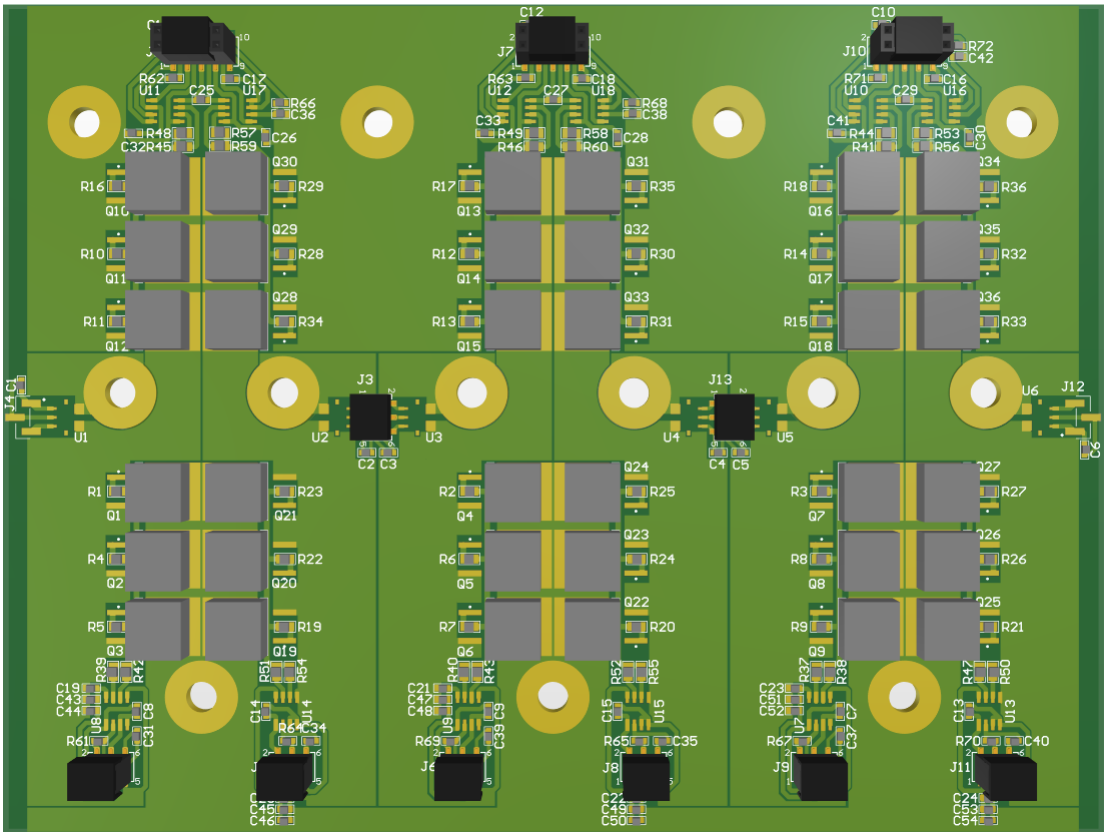

Figure 9: Lower PCB design

Upper PCB

The top layer for the upper PCB can be seen in figure 10 and the bottom layer can be seen in figure 11.

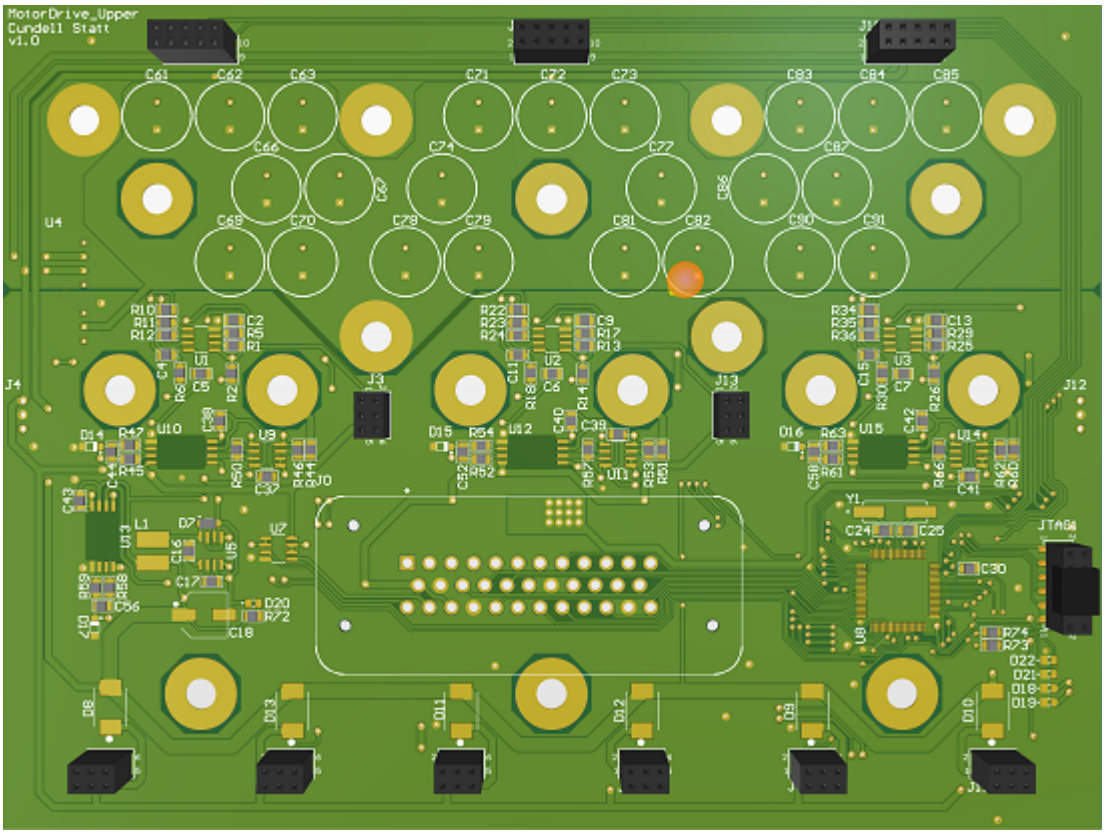

Figure 10: Upper PCB design top layer

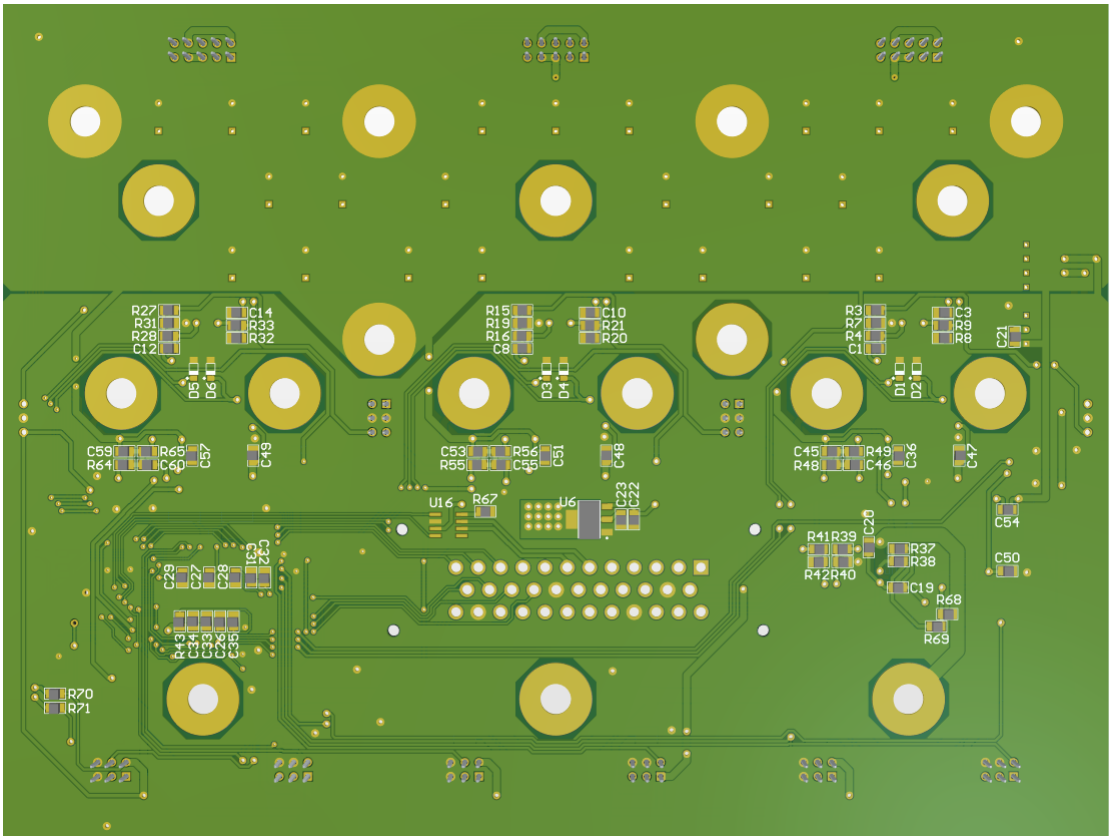

Figure 11: Upper PCB design bottom layer

Appendix C

Final PMSM drive built

The final PCB after construction can be seen in figures 12 to 14 .

Figure 12: Lower PCB top view

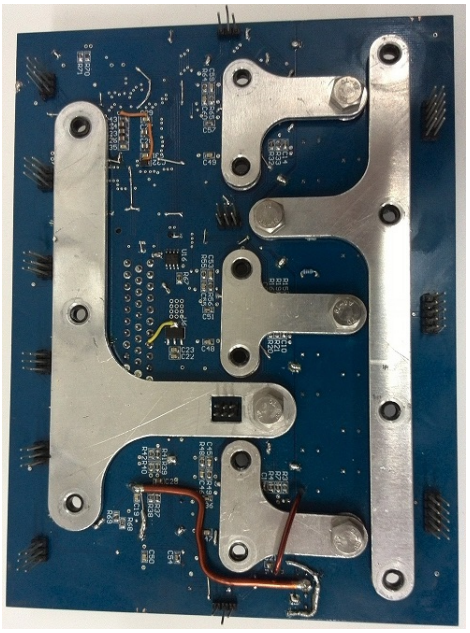

Figure 13: Upper PCB top view

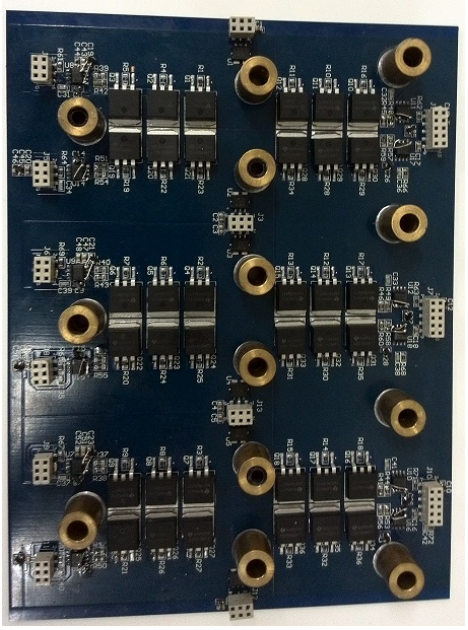

Figure 14: Upper PCB bottom view